NEW PRODUCT BRIEF

PERICOM®

CONNECTIVITY SOLUTIONS

PI7C9X2G304SLBQ

Gen2 PCIe® 3-Port/4-Lane SlimLine™ Packet Switch

The PI7C9X2G304SLBQ is a PCI Express® 2.1 3-port/4-lane PCI Express SlimLine™ Packet Switch specifically designed to meet automotive grade specification and the latest low-power, lead (Pb)-free, green system requirements. The PI7C9X2G304SLBQ is a high-performance, cost-effective solution that can be implemented in systems such as automotive system, embedded, Wi-Fi router/ gate-way, peripheral, storage, combo card, HBA, set-top box, moth-erboard and other power-sensitive high performance platforms. The name of the family, SlimLine™, refers to Pericom's proprietary power-saving PowerSave™ technology.

The PI7C9X2G304SLBQ provides one x1 or x2 upstream port and two x1 downstream ports. The PI7C9X2G304SLBQ provides users the flexibility to expand or fan-out from a wide range of I/O Bridges such as PCH, ICH, IOH, embedded MCU, FPGA, and other application specific ICs.

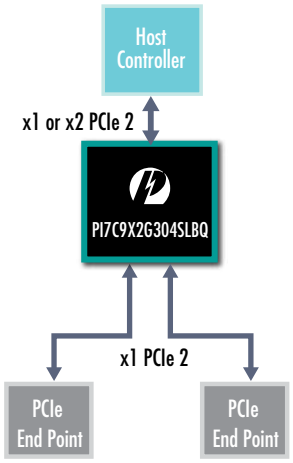
Industry Specifications Compliance

PCI Express® Base Specification, Revision 2.1

- PCI Express CEM Specification, Revision 2.0
- PCI-to-PCI Bridge Architecture Spec., Rev 1.2
- Advanced Configuration Power Interface (ACPI) Specification
- AECQ-100, Grade 3

Applications

- Automotive
- Wire/ Wireless Tele/ data communication
- Embedded system
- Set-top box and consumer devices
- Industrial control
- NAS/ Storage
- Peripheral
- PCIe Surveillance and Combo cards
- PC Motherboard PCIe slot expansion
- Set-top box and consumer devices



Ordering Information

Part Number	Package	PB-Free & Green	AECQ-100
PI7C9X2G304SLBQFDEX†	128 LQFP	YES	Grade 3
PI7C9X2G304SLBQEVB-X1U	Board	Evaluation kit offor PI7C9X2G-304SLBQ with x1 PCIe uplink	
PI7C9X2G304SLBQEVB-X2U	Board	Evaluation kit offor PI7C9X2G-304SLBQ with x2 PCIe uplink	

† Note: Adding an X suffix =Tape/Reel

Features

- PCISIG PCI Express 2.1 certificated
- Integrated 100MHz clock buffer for each downstream port
- Reliability, Availability and Serviceability
  - Supports Data Poisoning and End-to-End CRC
  - Advanced Error Reporting and Logging
  - IEEE 1149.6 JTAG interface support
- Link Power Management
  - Supports L0, L0s, L1, L2, L2/L3Ready and L3 link power state
  - Active state power management for L0s and L1 state
- Device State Power Management
  - Supports D0, D3Hot and D3Cold
  - 3.3V Aux Power support in D3Cold power state
- Supports up to 512-byte maximum payload size
- Power Dissipation: 0.65 W typical in L0 normal mode and 0.2W typical in L1 mode
- Industrial Temperature Range: -40°C to 85°C
- MTBF: 50,927,360 hours
- Package: 128-pin LQFP 14mm x 14mm
  - Pb free and 100% Green

Enhanced Features

- Programmable driver current and De-Emphasis Level at each individual port
- 150ns typical latency for packet running through switch without blocking
- Supports "Cut-through"(Default) as well as "Store and Forward" mode for switching packets
- Advanced Power Savings
  - Empty downstream ports are set to idle
  - Clock to corresponding circuit is turned off when any port enters L1 or ASPM L1
  - Supports Access Control Service (ACS) for peer-to-peer traffic
  - Supports Address Translation (AT) packet for SR-IOV application
  - Supports Latency Tolerance Reporting (LTR) to improve Platform Power Management
  - o Supports Optimized Buffer Flush Fill (OBFF) to improve Platform Power Management