Innovative Service Around the Globe YAGEO

DATA SHEET

SURFACE-MOUNT CERAMIC MULTILAYER CAPACITORS

C-Array: Class 1, NP0

50 V

size 0508 (4 × 0402)

Phycomp

Product Specification – Oct 29, 2003 V.7

Surface-mount ceramic multilayer capacitors

C-Array: Class 1, NP0 50 V size 0508 (4 × 0402)

FEATURES

- 4 × 0402 capacitors (of the same capacitance value) per array
- Less than 50% board space of an equivalent discrete component
- High volumetric efficiency
- Dense dielectric layers
- Supplied in tape on reel or loose in bag
- Increased throughput by time saved in mounting
- Cost savings on manufacturing time.

APPLICATIONS

- Professional electronics
- High density consumer electronics
- Automotive.

DESCRIPTION

Each capacitor element consists of a rectangular block of ceramic dielectric in which a number of interleaved precious metal electrodes are contained. This structure gives rise to a high capacitance per unit volume.

The inner electrodes are connected to the two terminations, silver dipped with a barrier layer of plated nickel and finally covered with a layer of plated tin (NiSn). An outline of the structure is shown in Fig.1.

QUICK REFERENCE DATA

DESCRIPTION	VALUE
Rated voltage U_R (DC)	50 V
Capacitance range (E12 series)	10 pF to 270 pF
Tolerance on capacitance	±5%, ±10%
Test voltage (DC) for 1 minute	2.5 × U_R
Sectional specifications	IEC 60384-10, second edition 1989-04; also based on CECC 32 100
Detailed specification	based on CECC 32 101-801
Climatic category (IEC 60068)	55/125/56

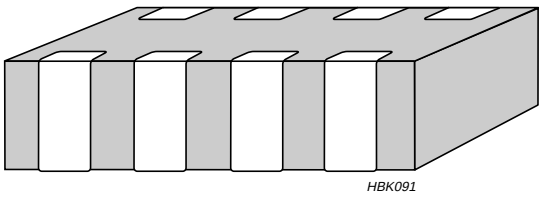
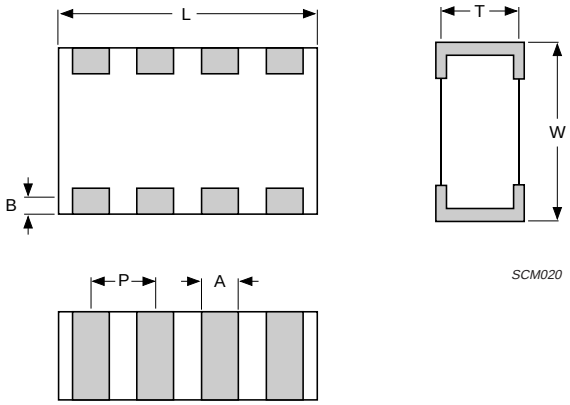


Fig.1 Simplified outline.

MECHANICAL DATA



For dimensions see Table 1.

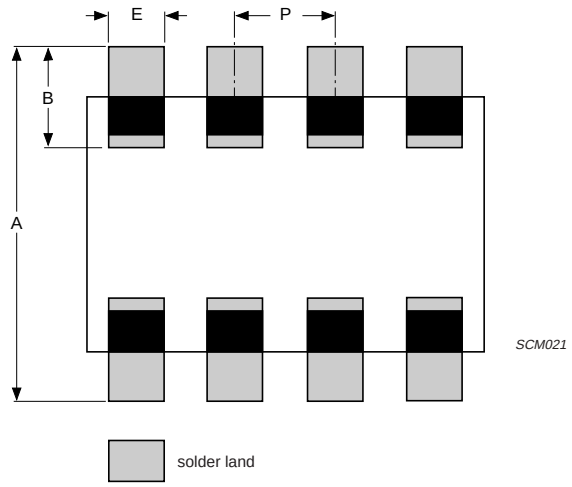
Fig.2 Dimensional outline.

Physical dimensions

Table 1 Capacitor dimensions for product size 0508 (4 × 0402)

CASE SIZE	L	W	T	A	B	P
Dimensions in millimetres						
0508 (4 × 0402)	2.0 ±0.15	1.25 ±0.15	0.60 ±0.10	0.28 ±0.10	0.2 ±0.10	0.50 ±0.10

DIMENSIONS OF SOLDER LANDS



For dimensions see Table 2.

Fig.3 Recommended dimensions of solder lands.

Table 2 Solder land dimensions; see Fig.3

CASE SIZE	FOOTPRINT DIMENSIONS (mm)			
	A	B	P	E
0508 (4 × 0402)	2.0 +0.40/–0.20	0.31 ±0.10	0.50±0.10	0.30 +0.02/–0.05

SELECTION CHART FOR 50 V

C (pF)	LAST TWO DIGITS OF 12NC	50 V
		0508 (4 × 0402)
10	23	
12	24	
15	25	
18	26	
22	27	
27	28	
33	29	
39	31	
47	32	0.6 ±0.1
56	33	
68	34	
82	35	
100	36	
120	37	
150	38	
180	39	
220	41	
270	42	

Note

1. Values in shaded cells indicate thickness class.

Thickness classification and packing quantities

THICKNESS CLASSIFICATION (mm)	8 mm TAPE WIDTH QUANTITY PER REEL
	∅180 mm; 7"
	PAPER
0.6 ±0.1	4 000

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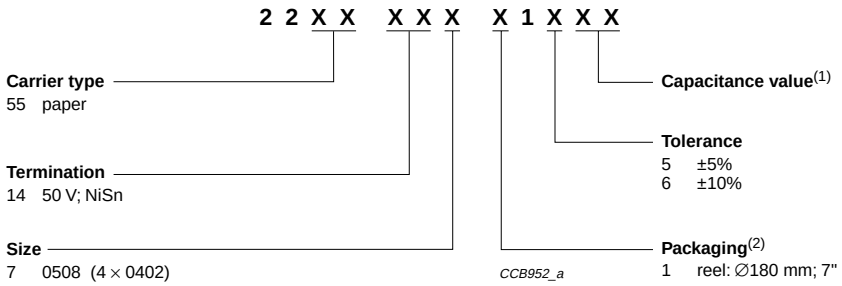
C-Array: Class 1, NP0 50 V size 0508 (4 × 0402)

ORDERING INFORMATION

Components may be ordered by using either a Phycomp's unique 12NC or simple 15-digit clear text code.

Ordering code 12NC (preferred)



(1) Refer to chapter "Selection chart".

(2) Quantity on reel depends on thickness classification, see section "Thickness classification and packing quantities".

Clear text code

EXAMPLE: 0508CG820J9B100

Size Code	Temp. Char.	Capacitance	Tol.	Vol.	Termination	Packing	Marking	Series
0508 (4 × 0402)	CG = NP0	820 = 82 pF; the third digit signifies the multiplying factor: 0 = × 1 1 = × 10	J = ±5% K = ±10%	9 = 50 V	B = NiSn	2 = 180 mm; 7" paper	0 = no marking	0 = conv. ceramic

ELECTRICAL CHARACTERISTICS

Class 1 capacitors; NP0 dielectric; NiSn terminations

Unless otherwise stated all electrical values apply at an ambient temperature of 20 ±1 °C, an atmospheric pressure of 86 to 106 kPa, and a relative humidity of 63 to 67%.

DESCRIPTION	VALUE
Capacitance range (E12 series); note 1	10 pF to 270 pF
Tolerance on capacitance after 1000 hours	±5%; ±10%
Test voltage (DC) for 1 minute	$2.5 \times U_R$
Tan δ; note 1	≤ 0.1%
Insulation resistance after 1 minute at U_R (DC):	R_{ins} ≥100 GΩ
Temperature coefficient	$(0 \pm 30) \times 10^{-6}$/K
Resistance to soldering heat	260 °C; 10 seconds

Note

1. Measured at 1 V, 1 MHz 20 °C, using a four-gauge method.

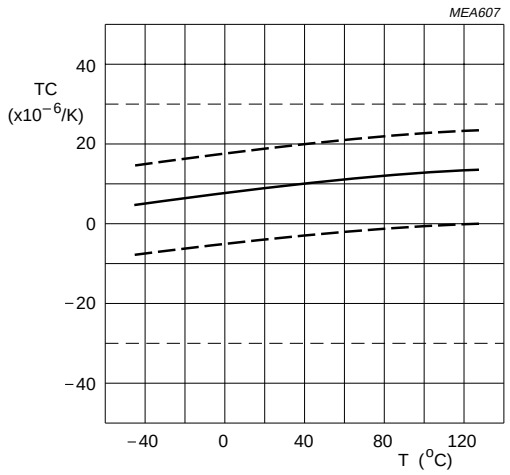


Fig.4 Typical temperature coefficient as a function of temperature.

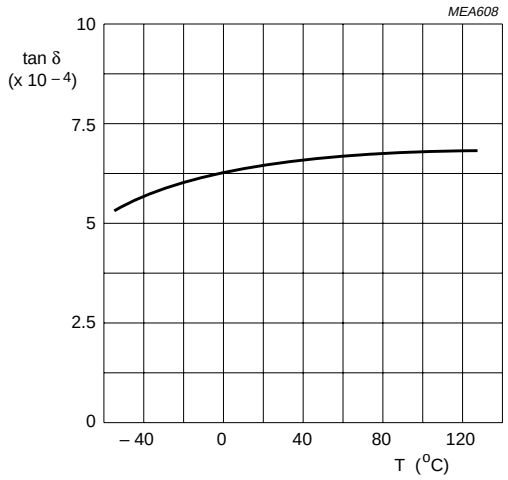


Fig.5 Typical tan δ as a function of temperature.

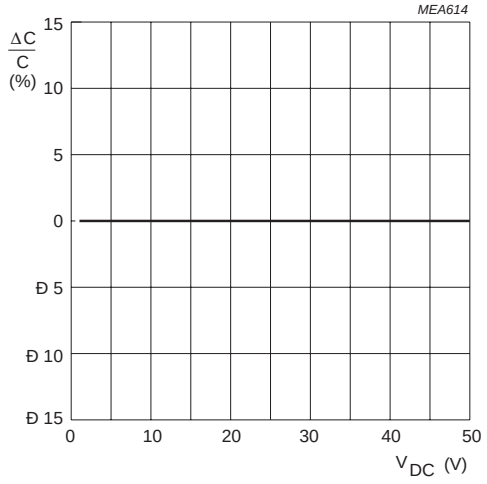


Fig.6 Typical capacitance change with respect to the capacitance at 1 V as a function of DC voltage.

TESTS AND REQUIREMENTS

Table 3 Test procedures and requirements

IEC 60384-10/ CECC 32 100 CLAUSE	IEC 60068-2 TEST METHOD	TEST	PROCEDURE	REQUIREMENTS
4.5		visual inspection and dimension check	any applicable method using ×10 magnification	in accordance with specification
4.6.1		capacitance	f = 1 MHz; measuring voltage 1 V_{rms} at 20 °C	within specified tolerance
4.6.2		tan δ	f = 1 MHz; measuring voltage 1 V_{rms} at 20 °C	in accordance with specification
4.6.3		insulation resistance	at U_R (DC) for 1 minute	in accordance with specification
4.6.4		voltage proof	2.5 × U_R for 1 minute	no breakdown or flashover
4.7.1		temperature coefficient	between minimum and maximum temperature	in accordance with specification
4.8		adhesion	a force of 5 N applied for 10 s to the line joining the terminations and in a plane parallel to the substrate	no visible damage
4.9		bond strength of plating on end face	mounted in accordance with CECC 32 100, paragraph 4.4	no visible damage
			conditions: bending 1 mm at a rate of 1 mm/s, radius jig 340 mm	ΔC/C: ±10%
4.10	Tb	resistance to soldering heat; jig clamps to the second component along the longitudinal direction	270 ±5 °C for 10 ±0.5 s in a static solder bath	the terminations shall be well tinned after recovery ΔC/C: within ±0.5% or 0.5 pF, whichever is greater
		resistance to soldering heat; jig clamps to the second component along the longitudinal direction	260 ±5 °C for 30 ±1 s in a static solder bath	using visual enlargement of ×10, dissolution of the terminations shall not exceed 10%
4.11	Ta	solderability; jig clamps to the second component along the longitudinal direction	zero hour test, and test after storage (20 to 24 months) in original packing in normal atmosphere; unmounted chips completely immersed for 3 ±0.5 s in a solder bath at 215 ±5 °C	the terminations shall be well tinned

IEC 60384-10/ CECC 32 100 CLAUSE	IEC 60068-2 TEST METHOD	TEST	PROCEDURE	REQUIREMENTS
4.12	Na	rapid change of temperature	−55 °C to +125 °C; 5 cycles	no visible damage after 24 hours recovery; $\Delta C/C$: within ±1% or 1 pF
4.14	Ca	damp heat	56 days at 40 °C; 90 to 95% RH; U_R applied	no visible damage after 24 hours recovery: $\Delta C/C$: within ±2% or 1 pF, whichever is greater tan δ: 2 ×specified value R_{ins}: 2500 MΩ or $R_i C_R \geq 25$ s, whichever is less
4.15		endurance	1000 hours at maximum temperature at 2 × U_R	after 24 hours recovery: $\Delta C/C$: within ±2% or 1 pF, whichever is greater tan δ: 2 ×specified value R_{ins}: 4000 MΩ or $R_i C_R \geq 40$ s, whichever is less

REVISION HISTORY

Revision	Date	Change Notification	Description
Rev.4	2001 May 30	-	- Converted to Phycomp brand
Rev.5	2003 Mar 13	-	- Updated company logo
Rev.6	2003 Jul 18	-	- Cover page revised
Rev.7	2003 Oct 29	-	- Physical dimension revised on size B