

PI6C5912012
12 Output LVPECL Fanout Buffer
Features

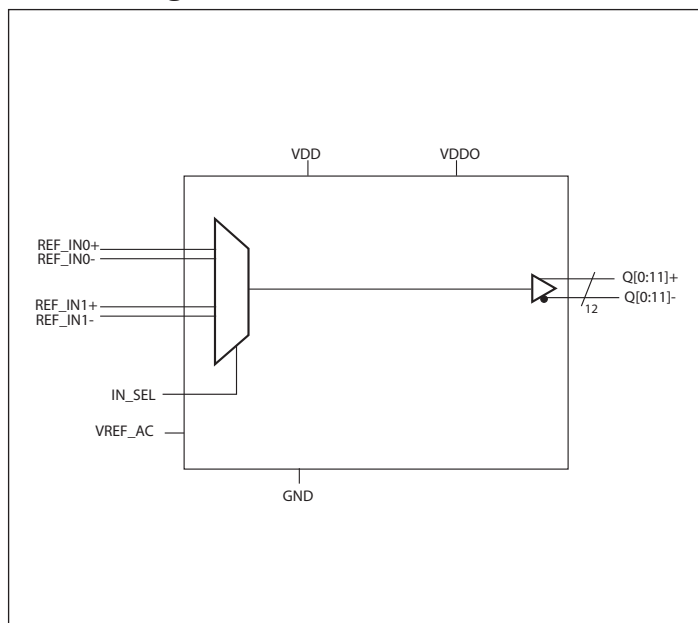
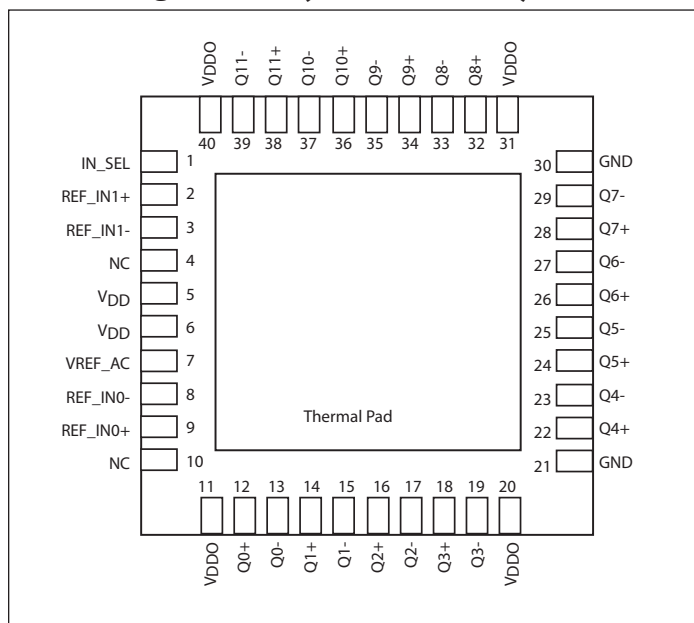
- 12 Differential LVPECL outputs
- 2 Selectable reference inputs support either single-ended or differential
- Up to 2GHz output frequency
- Ultra low additive phase jitter: < 0.01 ps (typ) (differential 156.25MHz, 12KHz to 20MHz integration range)
- Low skew between outputs
- Low delay from input to output
- Separate Input and output supply voltage for level shifting
- 2.5V / 3.3V power supply
- Industrial temperature support
- TQFN-40 package

Description

The PI6C5912012 is a high performance LVPECL fanout buffer device which supports up to 2GHz frequency. This device is ideal for systems that need to distribute low jitter LVPECL clock signals to multiple destinations.

Applications

- Networking systems including switches and routers
- High frequency backplane based computing and telecom platforms

Block Diagram

Pin Configuration (40-Pin TQFN)


Pin Description

Pin #	Pin Name	Type		Description
1	IN_SEL	Input	Pulldown	Input clock select. See Table 1 for function. LVCMOS/LVTTL interface levels.
2,3	REF_IN1+	Input		Reference input 1. Accepts Differential or Single Ended inputs
	REF_IN1-			
4, 10	NC	-		No Connect
5, 6	VDD	Power		Core power supply
7	VREF_AC	Output		Bias voltage output.
8, 9	REF_IN0-	Input		Reference input 0. Accepts Differential or Single Ended inputs
	REF_IN0+			
11, 20, 31, 40	VDDO	Power		Output power supply
12, 13	Q0+	Output		LVPECL output pair 0.
	Q0-			
14, 15	Q1+	Output		LVPECL output pair 1.
	Q1-			
16, 17	Q2+	Output		LVPECL output pair 2.
	Q2-			
18, 19	Q3+	Output		LVPECL output pair 3.
	Q3-			
21, 30	GND	Power		Power supply ground
22, 23	Q4+	Output		LVPECL output pair 4.
	Q4-			
24, 25	Q5+	Output		LVPECL output pair 5.
	Q5-			
26, 27	Q6+	Output		LVPECL output pair 6.
	Q6-			
28, 29	Q7+	Output		LVPECL output pair 7.
	Q7-			
32, 33	Q8+	Output		LVPECL output pair 8.
	Q8-			
34, 35	Q9+	Output		LVPECL output pair 9.
	Q9-			
36, 37	Q10+	Output		LVPECL output pair 10.
	Q10-			

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Pin Description Cont.

Pin #	Pin Name	Type	Description
38, 39	Q11+	Output	LVPECL output pair 11.
	Q11-		
Thermal pad	-	-	Thermal pad. Connect to ground.

Function Table

Table 1: Input select function

IN_SEL	Function
0 (default)	REF_IN0 is the selected reference input
1	REF_IN1 is the selected reference input

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance			2		pF
$R_{PULDDOWN}$	Input Pulldown Resistor			200		k Ω
R_{PULLUP}	Input Pullup Resistor			200		k Ω

Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested)

Storage temperature.....	-55 to +150°C
Supply Voltage to Ground Potential (V_{DD} , V_{DDO})...	-0.5 to +4.6V
Inputs (Referenced to GND)	-0.5 to $V_{DD}+0.5V$
Clock Output (Referenced to GND).....	-0.5 to $V_{DD}+0.5V$
Latch up	200mA
ESD Protection (Input)	2000 V min (HBM)
ESD Protection (Input)	1000 V min (CDM)

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Power Supply Characteristics and Operating Conditions

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{EE}	Supply Internal Current			89	105	mA
I_{DD}	Core Power Supply Current			69	80	
T_A	Ambient Operating Temperature		-40		85	°C

DC Electrical Specifications - Differential Inputs

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
I_{IH}	Input High current	Input = V_{DD}			85	uA
I_{IL}	Input Low current	Input = GND	-85			uA
V_{IH}	Input high voltage				$V_{DD}+0.3$	V
V_{IL}	Input low voltage		-0.3			V
V_{ID}	Input Differential Amplitude PK-PK		0.1			V
V_{CM}	Common mode input voltage		GND + 0.5		$V_{DD}-0.85$	V
ISO_{MUX}	MUX isolation			-89		dBc

DC Electrical Specifications - LVCMOS Inputs

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IH}	Input High current	Input = V_{DD}			50	μA
I_{IL}	Input Low current	Input = GND	-50			μA
V_{IH}	Input high voltage	$V_{DD}=3.3V$	2.0		$V_{DD}+0.3$	V
V_{IL}	Input low voltage	$V_{DD}=3.3V$	-0.3		0.8	V
V_{IH}	Input high voltage	$V_{DD}=2.5V$	1.7		$V_{DD}+0.3$	V
V_{IL}	Input low voltage	$V_{DD}=2.5V$	-0.3		0.7	V

DC Electrical Specifications- LVPECL Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High voltage		$V_{DDO}-1.4$		$V_{DDO}-0.9$	V
V_{OL}	Output Low voltage	$V_{DD}=2.5V$	$V_{DDO}-1.9$		$V_{DDO}-1.25$	V
		$V_{DD}=3.3V$	$V_{DDO}-2.2$		$V_{DDO}-1.25$	V

AC Electrical Specifications – Differential Inputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F_{IN}	Clock input frequency				2000	MHz
V_{INPP}	Differential Input peak to peak voltage	$1.5GHz \leq F_{IN} \leq 2 GHz$	0.2		1.5	V
		$F_{IN} \leq 1.5 GHz$	0.1		1.5	V
ER	Input Edge Rate		1.5			V/ns

AC Electrical Specifications – LVCMOS Inputs

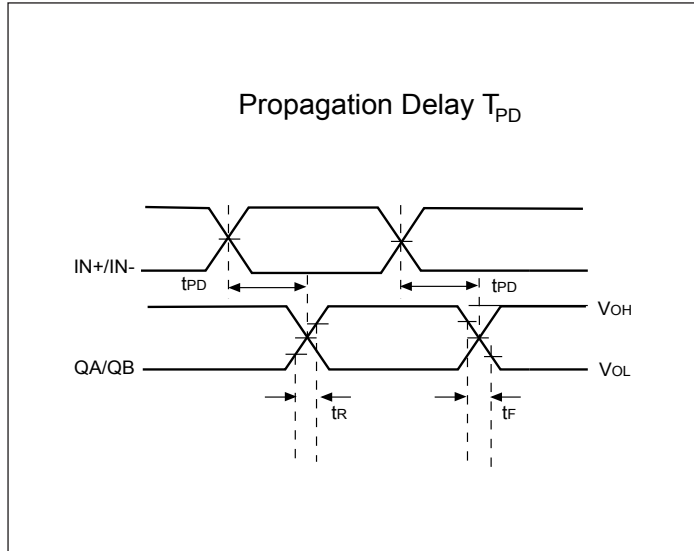
Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F_{IN}	Clock input frequency				200	MHz
V_{INPP}	Differential Input peak to peak voltage	$1.5GHz \leq F_{IN} \leq 2 GHz$	0.2		1.5	V
		$F_{IN} \leq 1.5 GHz$	0.1		1.5	V
ER	Input Edge Rate		1.5			V/ns

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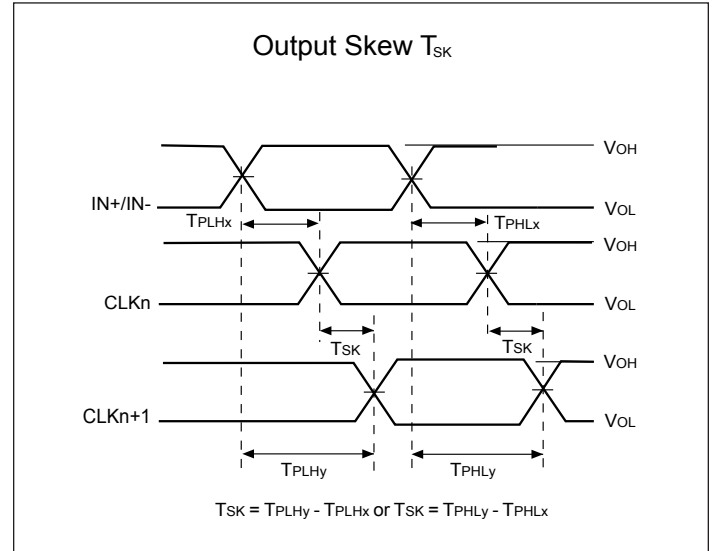
AC Electrical Specifications – LVPECL Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F _{OUT}	Clock output frequency	LVPECL			2000	MHz
T _r	Output rise time	From 20% to 80%		150		ps
T _f	Output fall time	From 80% to 20%		150		ps
T _{ODC}	Output duty cycle		48		52	%
V _{PP}	Output swing Single-ended	@1GHz to ≤2GHz	250		850	mV
		@ ≤1GHz	500		950	mV
T _j	Buffer additive jitter RMS	156.25MHz, 12kHz to 20MHz		0.01		ps
		156.25MHz, 10kHz to 1MHz		0.01		ps
T _{SK}	Output Skew			13	30	ps
T _{PD}	Propagation Delay				750	ps
T _{OD}	Valid to HiZ				100	ns
T _{OE}	HiZ to valid				100	ns
T _{P2P Skew}	Part to Part Skew ¹		-50		50	ps
V _{REF_AC}	Input bias voltage	I _{AC} = 2mA	V _{DD} -1.6		V _{DD} -1.1	V

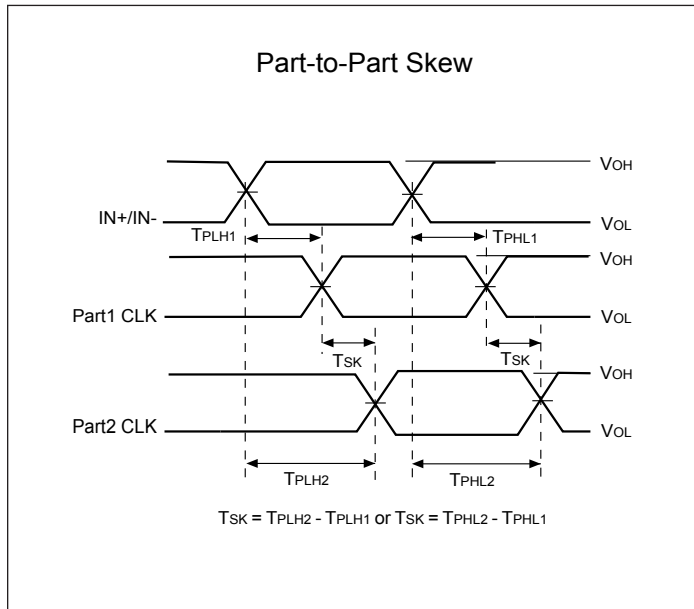
Propagation Delay



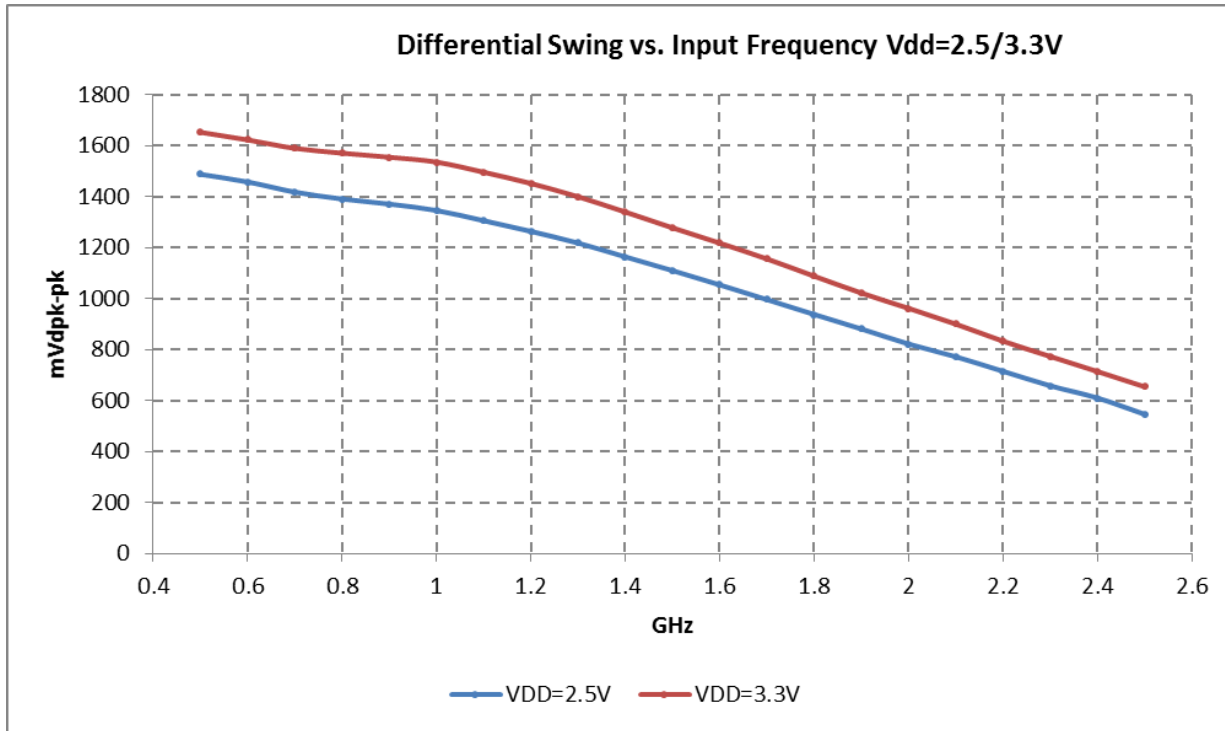
Output Skew



Part to Part Skew



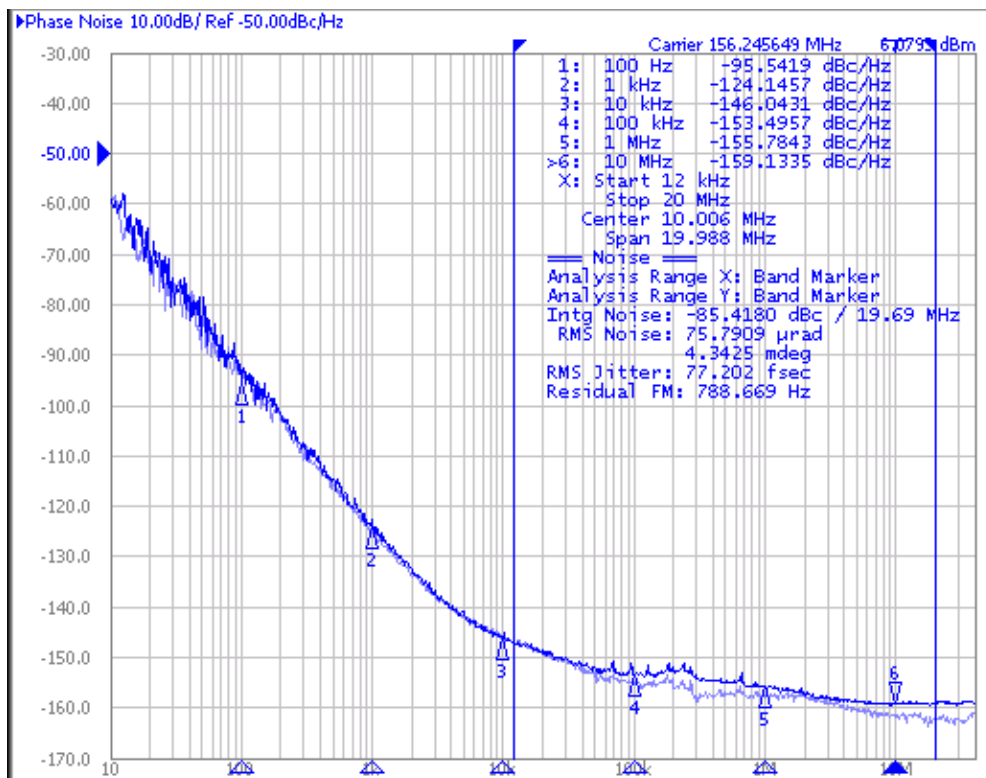
LVPECL Output Swing vs. Frequency



Phase Noise and Additive Jitter

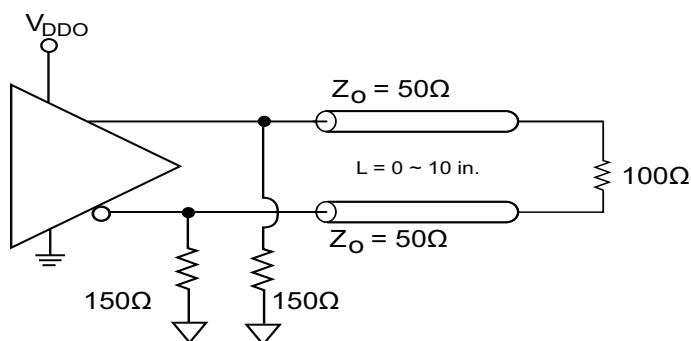
Output phase noise (Dark Blue) vs Input Phase noise (light blue)

$$\text{Additive jitter} = \sqrt{(\text{Output jitter}^2 - \text{Input jitter}^2)}$$



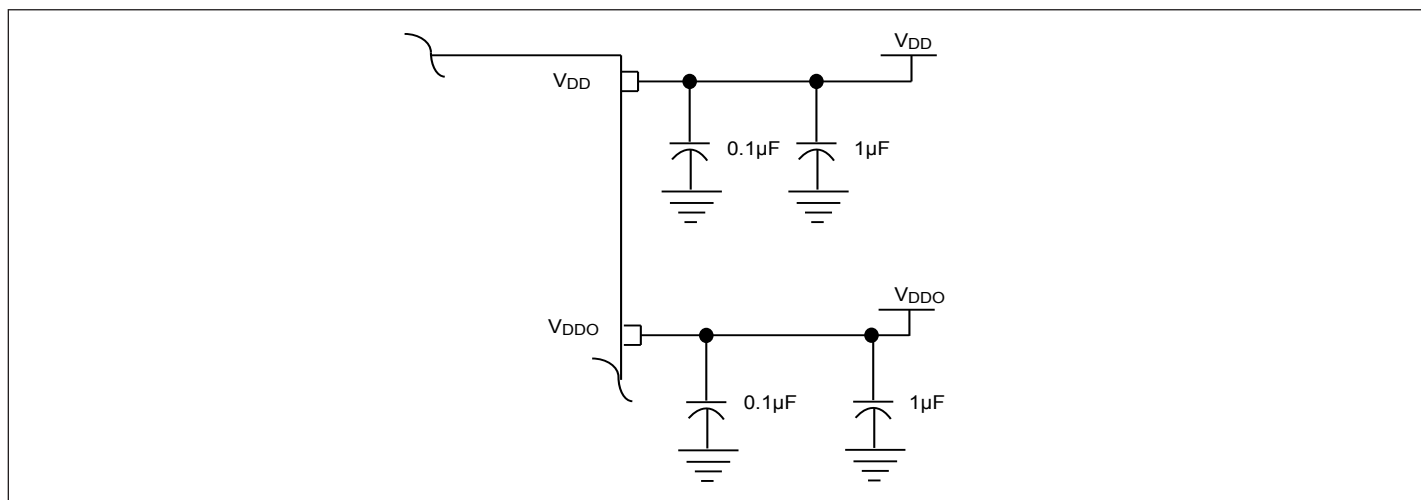
Configuration Test Load Board Termination for LVPECL/ LVDS Outputs

LVPECL Buffer



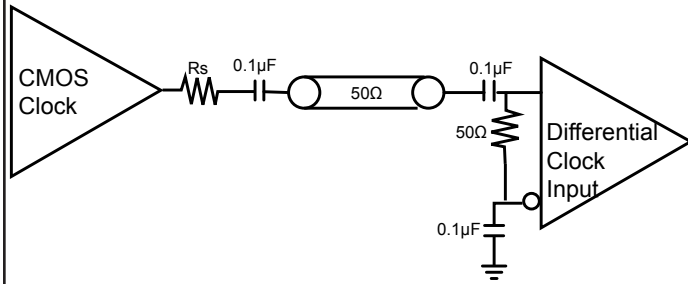
Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. All power pins should be individually connected to the power supply plane through vias, and 0.1 μ F and 1 μ F bypass capacitors should be used for each pin.

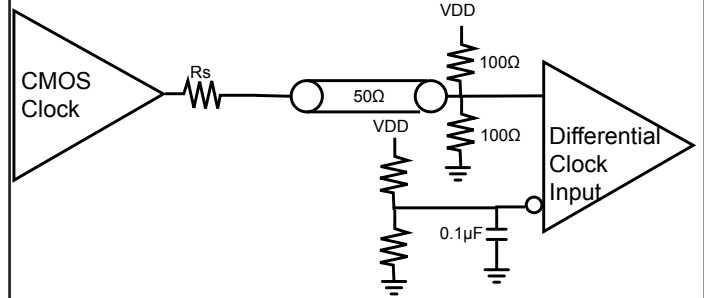


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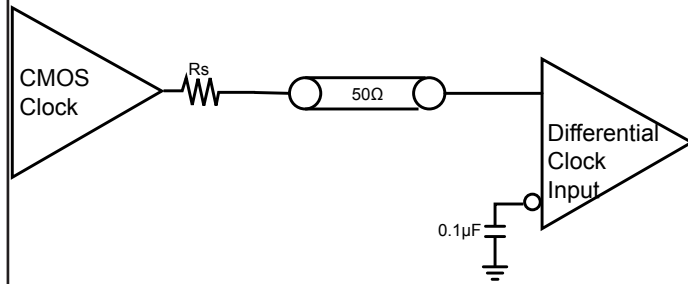
Single Ended Input, AC couple



Single Ended Input, DC couple

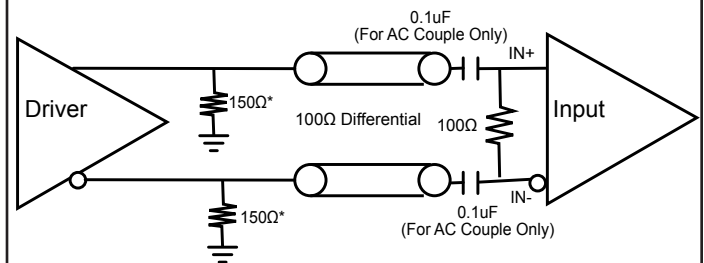


Single Ended Input, DC couple

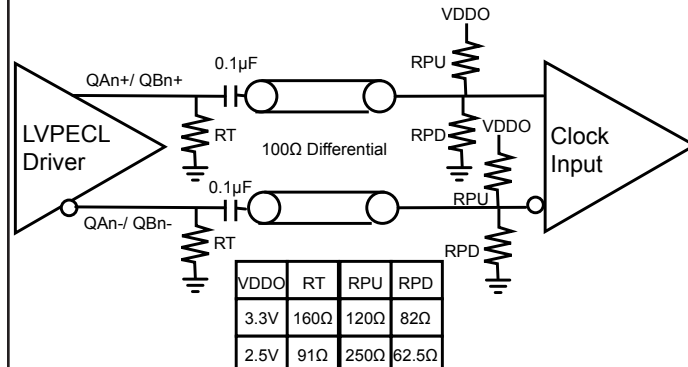


LVPECL/ LVDS AC and DC input

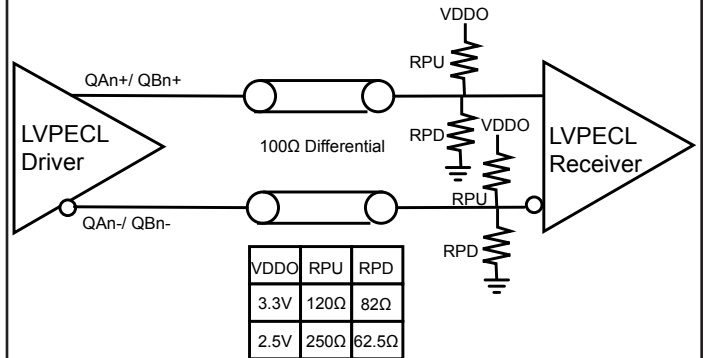
*Remove for LVDS



LVPECL, AC Couple, Thevenin Equivalent

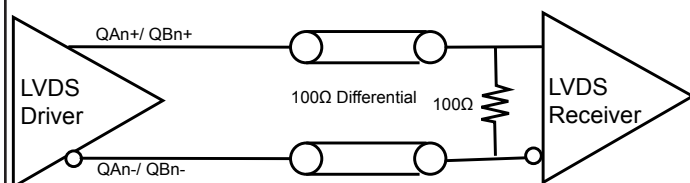


LVPECL, DC Couple, Thevenin Equivalent

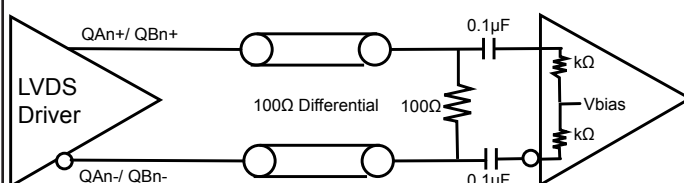


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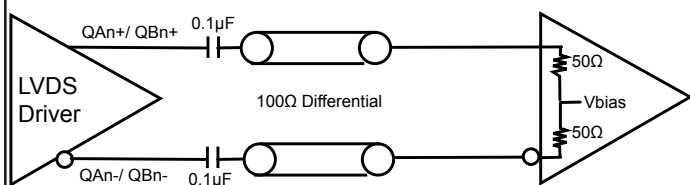
LVDS DC Couple



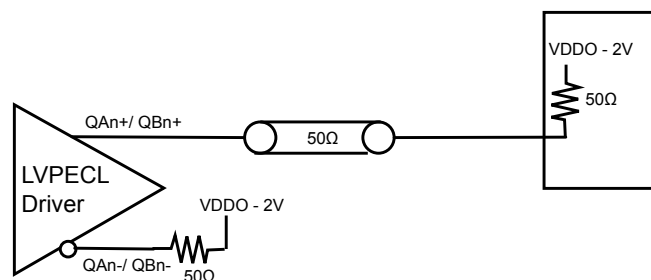
LVDS AC Couple at Load



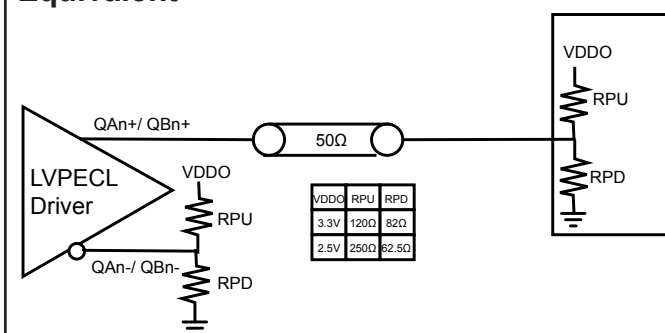
LVDS AC Couple with Internal Termination



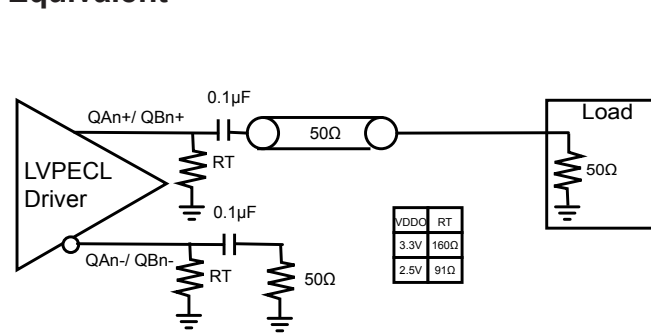
Single Ended LVPECL, DC Couple



Single Ended LVPECL, DC Couple, Thevenin Equivalent



Single Ended LVPECL, AC Couple, Thevenin Equivalent

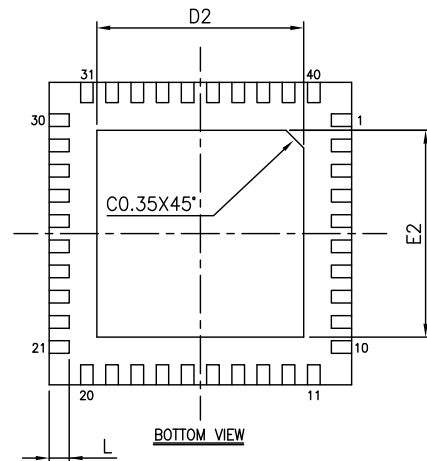
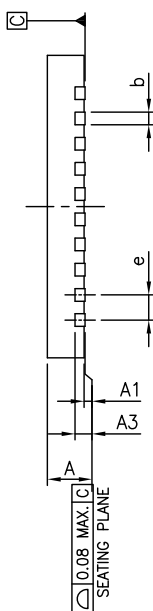
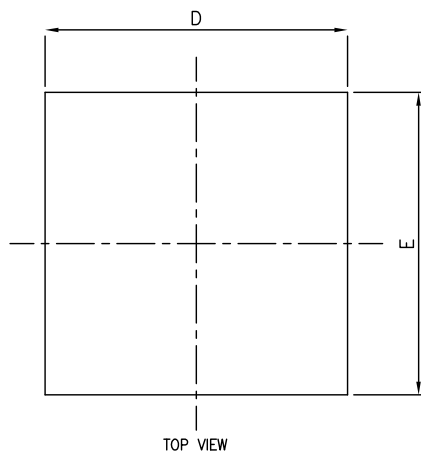


Thermal Information

Symbol	Description	Condition	
Θ_{JA}	Junction-to-ambient thermal resistance	Still air	26.18 °C/W
Θ_{JC}	Junction-to-case thermal resistance		10.52 °C/W

Part Marking

Top mark not available at this time. To obtain advance information regarding the top mark, please contact your local sales representative.

PI6C5912012
Packaging Mechanical: 40-TQFN (ZD)


SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.18	0.25	0.30
D	5.90	6.00	6.10
E	5.90	6.00	6.10
e	0.50 BSC		
L	0.35	0.40	0.45
D2	4.40	4.50	4.55
E2	4.40	4.50	4.55

Notes:

1. All dimensions are in mm.
2. Refer JEDEC MO-220.
3. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.



DATE: 07/12/11

DESCRIPTION: 40-contact, Thin Fine Pitch Quad Flat No-Lead, TQFN

PACKAGE CODE: ZD (ZD40)

DOCUMENT CONTROL #: PD-2021

REVISION: C

For latest package info.

 please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>
Ordering Information

Ordering Code	Package Code	Package Type	Operating Temperature
PI6C5912012ZDIEX	ZD	40-contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)	-40 °C to 85 °C

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <http://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free. Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
3. E = Pb-free and Green
4. X suffix = Tape/Reel

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