Sipeed USB-JTAG/TTL RISC-V Debugger (ST-Link V2 STM8/STM32 Simulator)

SKU 114991786

Sipeed USB-JTAG/TTL RISC-V Debugger (ST-Link V2 STM8/STM32 Simulator)

- 1 + CN Warehouse

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Support the full range of STM32 SWD debugging interface, a simple 4-wire interface (including power), fast, stable; interface definition housing directly marked! No need to read the manual

Support the full range of STM8 SWIM download debugging (common development environments such as IAR, STVD etc. are supported); supported software versions as follows:

- ST-LINK Utility 2.0 and 4.2.1 above
- STVD and above
- STVP 3.2.3 and above
- IAR EWARM V6.20 and above
- IAR EWSTM8 V1.30 and above
- KEIL RVMDK V4.21 and above

Support for automatic firmware upgrades to ensure follow-up support ST products. The factory firmware has been upgraded to the latest V2.J17.S4;

Increase the 5V power output, the output I / O ports are protected afraid of operational errors caused by ST-LINK V2 damage!

The interface easy to use copper gilded horns seat pitch of 2.54, with 20CM DuPont line, the line can respond to different target sequence, flexible wiring;

The use of U disk aluminum housing protects the motherboard, easy to carry, is not afraid of static electricity, afraid to fall throw touch.

Technical Details

Size: 54 x 20 x 9 mm

Part List

Sipeed USB-JTAG/TTL RISC-V Debugger x 1
DuPont Cable x 1

ECCN/HTS

ECCN	EAR99
HSCODE	8543709990

Bundle Sales

This item: Sipeed USB-JTAG/TTL RISC-V Debugger (ST-Link V2 STM8/STM32 Simulator)
Sipeed TANG PriMER FPGA Development Board