PFE1500-12-054xD Series

DC-DC Front End Power Supply

The PFE1500-12-054xD is 1500 watt DC to DC power supply that converts DC input into a main output of 12 VDC for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches.

The PFE1500-12-054xD meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).

RoHS Compliant

Key Features & Benefits

- High Efficiency, typ. 94% efficiency at half load
- Wide input voltage range: 40 – 72 VDC
- Always-On standby output (model dependent):
  - Programmable 3.3 V / 5 V (16.5 W)
  - 12 V @ 3 A (36 W)
- Hot-plug capable
- Parallel operation with active digital current sharing
- High density design: 35 W/in^3
- Small form factor: 321.5 x 54.5 x 40 mm (12.66 x 2.14 x 1.57 in)
- I^{2}C communication interface for control, programming and monitoring with Power Management Bus protocol
- Over temperature, output overvoltage and overcurrent protection
- 256 Bytes of EEPROM for user information
- 2 Status LEDs: IN OK and OUT OK with fault signaling

Applications

- High Performance Servers
- Routers
- Switches

1. ORDERING INFORMATION

MODELS WITH PROGRAMMABLE 3.3 V / 5 V STANDBY OUTPUT*

PFE	1500	-	12	-	054	X	D
Product Family	**Power Level**	**Dash**	**V1 Output**	**Dash**	**Width**	**Airflow**	**Input**
PFE Front-Ends	1500 W		12 V		54 mm	N: Normal R: Reverse	DC

* Consult factor for availability.

MODELS WITH 12 V STANDBY OUTPUT

PFE	1500	-	12	x	D	S412
Product Family	**Power Level**	**Dash**	**V1 Output**	**Airflow**	**Input**	**VSB Output**
PFE Front-Ends	1500 W		12 V	N: Normal air flow R: Reverse air flow	DC	12VSB

2. OVERVIEW

The PFE1500-12-054xD DC/DC power supply is a DSP controlled, high efficient front-end power supply. It incorporates state of the art technology and uses an interleaved forward converter topology with active clamp and synchronous rectification to reduce component stresses, thus providing increased system reliability and very high efficiency. With a wide input DC voltage range the PFE1500-12-054xD maximizes power availability in demanding server, network, and other high availability applications. The supply is fan cooled and ideally suited for integration with a matching airflow path.

An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems.

The always-on standby output provides power to external power distribution and management controllers. It is protected with an active OR-ing device for maximum reliability.

Status information is provided with a front-panel LED. In addition, the power supply can be controlled and the fan speed set via the I2C bus. The I2C bus allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures. Cooling is managed by a fan controlled by the DSP controller. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I2C bus.

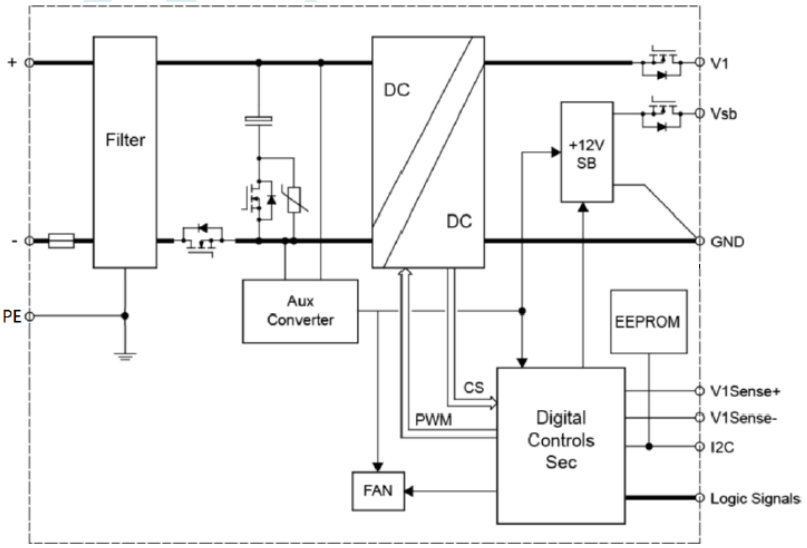


Figure 1. Block Diagram

3. ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the supply.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Vi *maxc*	Maximum Input Voltage	Continuous			75	VDC

4. INPUT SPECIFICATIONS

General Condition: T_A = 0… 45°C unless otherwise specified.

PARAMETER		CONDITIONS / DESCRIPTION	MIN	NOM	MAX	UNIT
$V_{i\,nom}$	Nominal input voltage			53		VDC
V_i	Input voltage ranges	Normal operating ($V_{i\,min}$ to $V_{i\,max}$)	40		72	VDC
$I_{i\,max}$	Max input current				45	A_{rms}
$I_{i\,p}$	Inrush Current Limitation	$V_{i\,min}$ to $V_{i\,max}$			70	A_p
$V_{i\,on}$	Turn-on input voltage[1]	Ramping up	42		45	VDC
$V_{i\,off}$	Turn-off input voltage[1]	Ramping down	37		40	VDC
η	Efficiency without fan	$V_{i\,nom}$, 0.1·$I_{x\,nom}$, $V_{x\,nom}$, T_A = 25 °C		82		%
		$V_{i\,nom}$, 0.2·$I_{x\,nom}$, $V_{x\,nom}$, T_A = 25 °C		90		
		$V_{i\,nom}$, 0.5·$I_{x\,nom}$, $V_{x\,nom}$, T_A = 25 °C		94		
		$V_{i\,nom}$, $I_{x\,nom}$, $V_{x\,nom}$, T_A = 25 °C		91		
T_{hold}	Hold-up Time	V_i > 10.8 V, V_{SB} within regulation, V_i = 53 VDC, P_{Onom} *(from DC input lost to V1 lost to 10.8V)*	2			ms

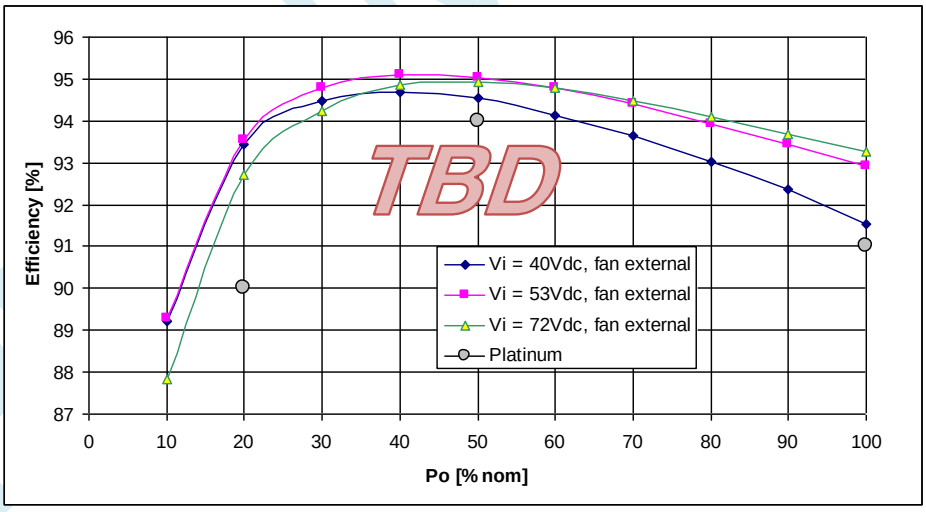


Figure 2. Efficiency Curve

[1] The Front-End is provided with a minimum hysteresis of 3 V during turn-on and turn-off within the ranges.

5. OUTPUT SPECIFICATIONS

General Condition: T_A = 0… 45°C unless otherwise specified.

PARAMETER		CONDITIONS / DESCRIPTION		MIN	NOM	MAX	UNIT
Main Output V_1							
$V_{1\ nom}$	Nominal Output Voltage	0.5 · $I_{1\ nom}$, T_{amb} = 25 °C			12.0		VDC
$V_{1\ set}$	Output Setpoint Accuracy			-0.5		+0.5	% $V_{1\ nom}$
d $V_{1\ tot}$	Total Regulation	$V_{1\ min}$ to $V_{1\ max}$, 0 to 100% $I_{1\ nom}$, $T_{a\ min}$ to $T_{a\ max}$		-5		+5	% $V_{1\ nom}$
$P_{1\ nom}$	Nominal Output Power	V_1 = 12 VDC			1500		W
$I_{1\ nom}$	Nominal Output Current	V_1 = 12 VDC			125		ADC
$v_{1\ pp}$	Output Ripple Voltage	$V_{1\ nom}$, $I_{1\ nom}$, 20 MHz BW, 10nF/16V/X7R/1210 + 10uF/16V at V_1				150	mVpp
d $V_{1\ Load}$	Load Regulation	V_1 = $V_{1\ nom}$, 0 - 100 % $I_{1\ nom}$				480	mV
d $V_{1\ Line}$	Line Regulation	V_1 = $V_{1\ min}$... $V_{1\ max}$				150	mV
$I_{1\ max}$	Current Limitation			128		140	ADC
d I_{share}	Current Sharing	Deviation from $I_{1\ tot}$ / N, I_1 > 20%		-5		+5	%
d V_{dyn}	Dynamic Load Regulation	ΔI_1 = 50% $I_{1\ nom}$, I_1 = 5 … 100% $I_{1\ nom}$, dI_1/dt = 1 A/µs, recovery within 1% of $V_{1\ nom}$		-0.6		0.6	V
T_{rec}	Recovery Time				2		ms
$T_{DC\ V1}$	Start-Up Time From DC	V_1 = 10.8 VDC				2	sec
$t_{V1\ rise}$	Rise Time	V_1 = 10…90% $V_{1\ nom}$		1		70	ms
C_{Load}	Capacitive Loading	T_a = 25 °C				10 000	µF
3.3 / 5 V_{SB} ***Standby Output***							
$V_{SB\ nom}$	Nominal Output Voltage	0.5 · $I_{SB\ nom}$, T_{amb} = 25°C	VSB_SEL = 1		3.3		VDC
$V_{SB\ set}$	Output Setpoint Accuracy		VSB_SEL = 0		5.0		VDC
			VSB_SEL = 0 / 1	-0.5		+0.5	% V_{1nom}
$dV_{SB\ tot}$	Total Regulation	$V_{1\ min}$ to $V_{1\ max}$, 0 to 100% $I_{SB\ nom}$, $T_{a\ min}$ to $T_{a\ max}$		-3		+3	% V_{SBnom}
$P_{SB\ nom}$	Nominal Output Power	V_{SB} = 3.3 VDC			16.5		W
		V_{SB} = 5.0 VDC			16.5		
$I_{SB\ nom}$	Nominal Output Current	V_{SB} = 3.3 VDC			5		ADC
		V_{SB} = 5.0 VDC			3.3		
$V_{SB\ pp}$	Output Ripple Voltage	$V_{SB\ nom}$, $I_{SB\ nom}$, 20 MHz BW (See Section 5.1)				100	mVpp
dV_{SB}	Droop	0 - 100 % $I_{SB\ nom}$	VSB_SEL = 1		67		mV
			VSB_SEL = 0		44		
$I_{SB\ max}$	Current Limitation	VSB_SEL = 1		5.25		6	ADC
		VSB_SEL = 0		3.45		4.3	
dV_{SBdyn}	Dynamic Load Regulation	ΔI_{SB} = 50% $I_{SB\ nom}$, I_{SB} = 5 … 100% $I_{SB\ nom}$, dI_o/dt = 0.5 A/µs, recovery within 1% of $V_{1\ nom}$		-3		3	% V_{SBnom}
T_{rec}	Recovery Time					250	µs
$T_{DC\ VSB}$	Start-up Time from DC	V_{SB} = 90% $V_{SB\ nom}$				2	sec
$t_{VSB\ rise}$	Rise Time	V_{SB} = 10…90% $V_{SB\ nom}$		0.5		30	ms
C_{Load}	Capacitive Loading	T_{amb} = 25°C				10000	µF

12 V_{SB} Standby Output						
$V_{SB\ nom}$	Nominal Output Voltage	0.5 · $I_{SB\ nom}$, T_{amb} = 25 °C		12		VDC
$V_{SB\ set}$	Output Setpoint Accuracy		-1		+1	% $V_{1\ nom}$
$dV_{SB\ tot}$	Total Regulation	$V_{1\ min}$ to $V_{1\ max}$, 0 to 100% $I_{SB\ nom}$, $T_{a\ min}$ to $T_{a\ max}$	-3		+3	% V_{SBnom}
$P_{SB\ nom}$	Nominal Output Power			36		W
$I_{SB\ nom}$	Nominal Output Current			3		ADC
$V_{SB\ pp}$	Output Ripple Voltage	$V_{SB\ nom}$, $I_{SB\ nom}$, 20 MHz BW,			120	mVpp
d V_{SB}	Droop	0 - 100 % $I_{SB\ nom}$		270		mV
$I_{SB\ max}$	Current Limitation		3.3		3.9	ADC
d V_{SBdyn}	Dynamic Load Regulation	ΔI_{SB} = 50% $I_{SB\ nom}$, I_{SB} = 5 … 100% $I_{SB\ nom}$, dI_o/dt = 0.5 A/µs, recovery within 1% of $V_{1\ nom}$	-5		+5	% V_{SBnom}
T_{rec}	Recovery Time			2		ms
$T_{DC\ VSB}$	Start-Up Time from DC Input	V_{SB} = 90% $V_{SB\ nom}$			2	sec
$t_{VSB\ rise}$	Rise Time	V_{SB} = 10…90% $V_{SB\ nom}$	4		20	ms
C_{Load}	Capacitive Loading	T_{amb} = 25 °C			1500	µF

6. PROTECTION SPECIFICATIONS

PARAMETER		DESCRIPTION / CONDITION		MIN	NOM	MAX	UNIT
F	Input Fuse (L)	Not user accessible, quick-acting (F)			60		A
$V_{1\ OV}$	OV Threshold V_1			13.3		14.5	VDC
$t_{OV\ V1}$	OV Latch Off Time V_1	V1 with half load			1		ms
$V_{SB\ OV}$	OV Threshold V_{SB}			13.3		14.5	VDC
$t_{OV\ VSB}$	OV Latch Off Time V_{SB}	Vsb with half load			1		ms
$I_{V1\ lim}$	Over Current Limitation V_1	T_a < 45°C		128		140	A
$I_{VSB\ lim}$	Over Current Limitation V_{SB}	T_a < 45°C for	3.3 V_{SB}	5.25		6	A
			5.0 V_{SB}	3.45		4.3	
			12 V_{SB}	3.3		3.9	
$I_{V1\ SC}$	Max Short Circuit Current V_1	V_1 < 3V				TBD	A
$t_{V1\ SC}$	Short Circuit Regulation Time	V_1 < 3 V, time until I_{V1} is limited to < $I_{V1\ sc}$				2	ms
T_{SD}	Over Temperature on Heat Sinks	Automatic shut-down			TBD		°C

6.1 OUTPUT GROUND

The output return path serves as power and signal ground. All output voltages and signals are referenced to these pins. To prevent a shift in signal and voltage levels due to ground wiring voltage drop a low impedance ground plane should be used as shown in *Figure 3*. Alternatively, separated ground signals can be used as shown in *Figure 4*. In this case the two ground planes should be connected together at the power supplies ground pins.

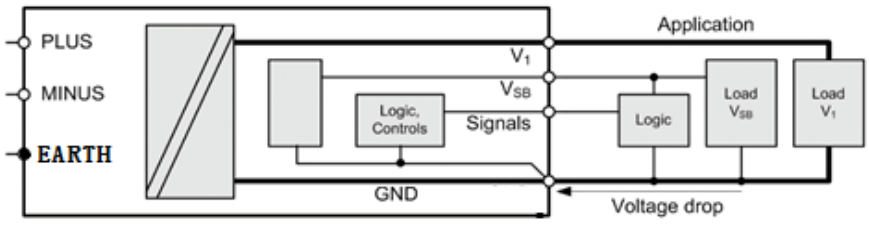


Figure 3. Common low impedance ground plane

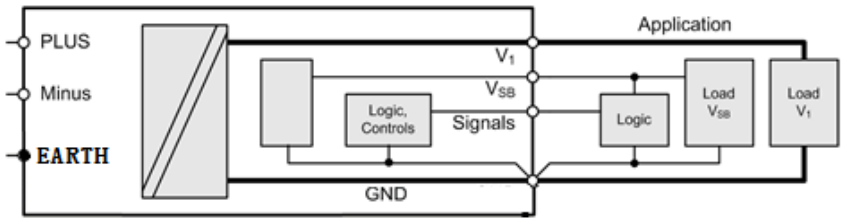


Figure 4. Separated power and signal ground

6.2 OVERVOLTAGE PROTECTION

The PFE front-ends provide a fixed threshold overvoltage (OV) protection implemented with a HW comparator. Once an OV condition has been triggered, the supply will shut down and latch the fault condition. The latch can be unlocked by disconnecting the supply from the DC mains or by toggling the PSON_L input.

6.3 VSB UNDERVOLTAGE DETECTION

LED and PWOK_L pin signal assert if the output voltage exceeds ±7% of its nominal voltage. Output under voltage protection is provided on both outputs. When either V_1 or V_{SB} falls below 93% of its nominal voltage, the output is inhibited.

6.4 CURRENT LIMITATION

6.4.1 MAIN OUTPUT

When main output runs in current limitation mode its output will turn OFF below 2 V but will retry to recover every 1 s interval. If current limitation mode is still present after the unit retry, output will continuously perform this routine until current is below the current limitation point. The supply will go through soft start every time it retry from current limitation mode.

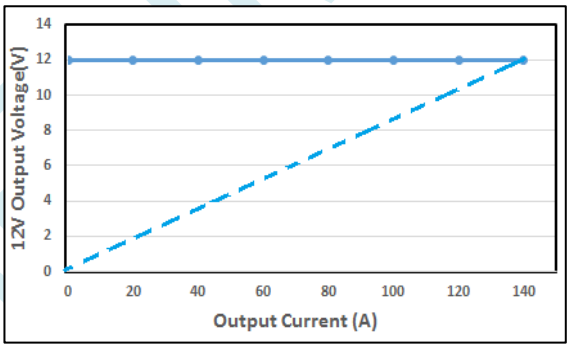


Figure 5. Current Limitation on V1

The main output current limitation will decrease if the ambient (inlet) temperature increases beyond 45°C. Note that the actual over current protection on V1 will begin at a current level approximately 5 A higher, *Figure 7*. (See also Chapter 9 Temperature and Fan Control for additional information.)

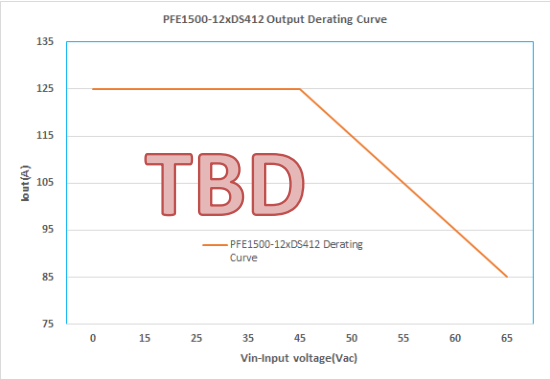


Figure 6. Iout Derating Curve for application above 45°C amb.

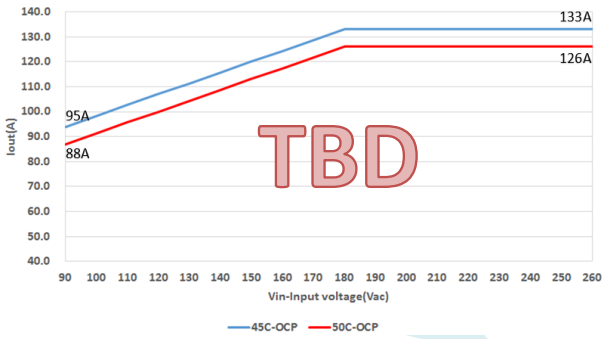


Figure 7. OCP Derating Curve with Ambient Temperature

6.4.2 STANDBY OUTPUT

3.3 / 5 V_{SB}

The standby output exhibits a substantially rectangular output characteristic down to 0 V (no hiccup mode / latch off). If it runs in current limitation and its output voltage drops below the UV threshold, then the main output will be inhibited (standby remains on). The current limitation of the standby output is independent of the DC input voltage.

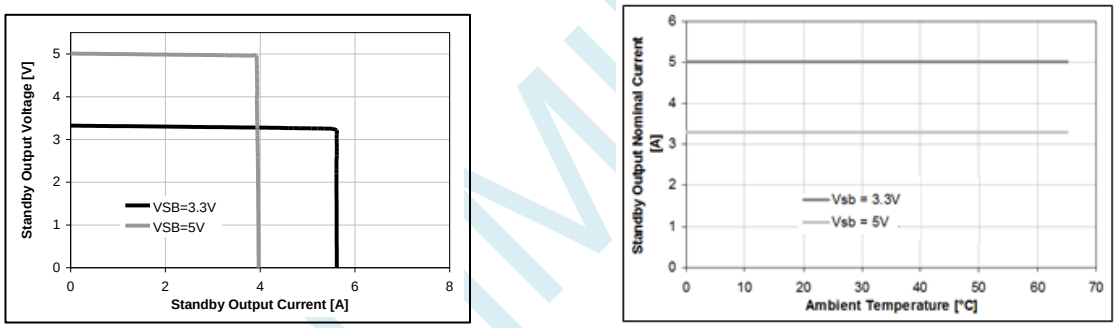


Figure 8. Current Limitation and Temperature Derating on 3.3 / 5 V_{SB}

12 V_{SB}

On the standby output, a hiccup type over current protection is implemented. This protection will shut down the standby output immediately when standby current reaches or exceeds $I_{VSB\ lim}$. After an off-time of 1s the output automatically tries to restart. If the overload condition is removed the output voltage will reach again its nominal value. At continuous overload condition the output will repeatedly trying to restart with 1s intervals. A failure on the Standby output will shut down both Main and Standby outputs.

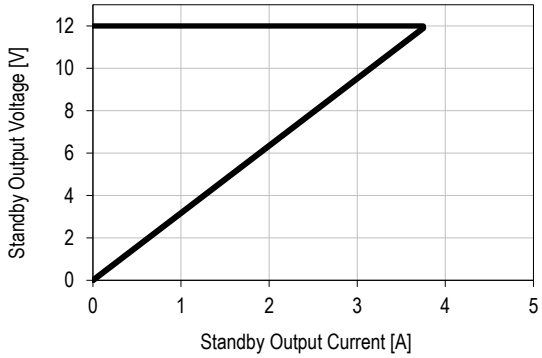


Figure 9. Current Limitation on 12 V_{SB}

7. MONITORING

PARAMETER	DESCRIPTION / CONDITION		MIN	NOM	MAX	UNIT
$V_{I\,mon}$	Input Voltage	$V_{I\,min} \le V_I \le V_{I\,max}$	-2		+2	VDC
$I_{I\,mon}$	Input Current		-1		+1	A
$P_{I\,mon}$	True Input Power	I1 > 25 A I1 ≤ 25 A	-5 -15		+5 15	% W
$V_{1\,mon}$	V_1 Voltage		-2		+2	%
$I_{1\,mon}$	V_1 Current	I1 > 25 A I1 ≤ 25 A	-2 -1.5		+2 +1.5	% A
$P_{o\,nom}$	Total Output Power	Po > 120 W Po ≤ 120 W	-5 -15		+5 +15	% W
$V_{SB\,mon}$	Standby Voltage		-0.3		+0.3	V
$I_{SB\,mon}$	Standby Current	$I_{SB} \le I_{SB\,nom}$	-0.5		+0.5	A

8. SIGNAL & CONTROL SPECIFICATIONS

8.1 ELECTRICAL CHARACTERISTICS

PARAMETER	DESCRIPTION / CONDITION		MIN	NOM	MAX	UNIT
PSKILL_H / PSON_L / VSB_SEL / HOTSTANDBYEN_H Inputs						
V_{IL}	Input Low Level Voltage		-0.2		0.8	V
V_{IH}	Input High Level Voltage		2.4		3.5	V
$I_{IL,\,H}$	Maximum Input Sink or Source Current		0		1	mA
$R_{puPSKILL\_H}$	Internal Pull Up Resistor on PSKILL_H			100		kΩ
R_{puPSON_L}	Internal Pull Up Resistor on PSON_L			10		kΩ
$R_{puHOTSTANDBYEN\_H}$	Internal Pull Up Resistor on HOTSTANDBYEN_H			10		kΩ
R_{LOW}	Resistance Pin to SGND for Low Level		0		1	kΩ
R_{HIGH}	Resistance Pin to SGND for High Level		50			kΩ
PWOK_H Output						
V_{OL}	Output Low Level Voltage	I_{sink} < 4 mA	0		0.4	V
V_{OH}	Output High Level Voltage	I_{source} < 0.5 mA	2.6		3.5	V
R_{puPWOK_H}	Internal Pull Up Resistor on PWOK_H			1		kΩ
VINOK_H Output						
V_{OL}	Output Low Level Voltage	I_{sink} < 2 mA	0		0.4	V
V_{OH}	Output High Level Voltage	I_{source} < 50 µA	2.6		3.5	V
$R_{puVINOK\_H}$	Internal Pull Up Resistor on VINOK_H			10		kΩ
SMB_ALERT_L Output						
V_{ext}	Maximum External Pull Up Voltage				12	V
V_{OL}	Output Low Level Voltage	I_{source} < 4 mA	0		0.4	V
I_{OH}	Maximum High Level Leakage Current				10	µA
$R_{puSMB\_ALERT\_L}$	Internal Pull Up Resistor on SMB_ALERT_L			None		kΩ

8.2 INTERFACING WITH SIGNALS

All signal pins have protection diodes implemented to protect internal circuits. When the power supply is not powered, the protection devices start clamping at signal pin voltages exceeding ±0.5 V. Therefore all input signals should be driven only by an open collector/drain to prevent back feeding inputs when the power supply is switched off.If interconnecting of signal pins of several power supplies is required, then this should be done by decoupling with small signal schottky diodes as shown in examples in *(Figure 10)* except for SMB_ALERT_L, ISHARE and I^2C pins. SMB_ALERT_L pins can be interconnected without decoupling diodes, since these pins have no internal pull up resistor and use a 15 V zener diode as protection device against positive voltage on pins. ISHARE pins must be interconnected without any additional components. This in-/output is disconnected from internal circuits when the power supply is switched off.

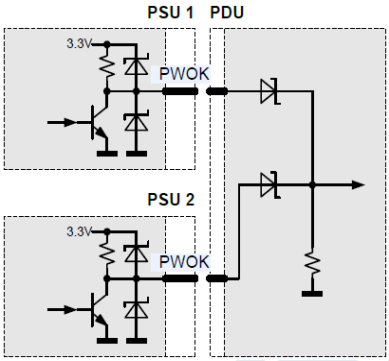


Figure 10. Interconnection of Signal Pins

8.3 FRONT LEDS

There will be 2 separate LED indicators, one green and one amber to indicate the power supply status. There will be a (slow) blinking green POWER LED (OK) to indicate that DC is applied to the PSU and the Standby Voltage is available. This same LED shall go steady to indicate that all the Power Outputs are available. This same LED or separate one will blink (slow) or be solid ON amber to indicate that the power supply has failed or reached a warning status and therefore a replacement of the unit is/maybe necessary. The LED are visible on the power supply's exterior face. The LED location meets ESD Requirements.

POWER SUPPLY CONDITION	GREEN (OK) LED STATUS	AMBER (FAIL) LED STATUS
No DC power to all power supplies	OFF	OFF
Power Supply Failure (includes over voltage, over current, over temperature and fan failure)	OFF	ON
Power Supply Warning events where the power supply continues to operate (high temperature, high power and slow fan)	OFF	Blinking
DC Present / V_{SB} on (PSU OFF)	Blinking	OFF
Power Supply ON and OK	ON	OFF

Table 1. LED Status

8.4 PRESENT_L

This signaling pin is recessed within the connector and will contact only once all other connector contacts are closed. This active-low pin is used to indicate to a power distribution unit controller that a supply is plugged in. The maximum current on PRESENT_L pin should not exceed 10 mA.

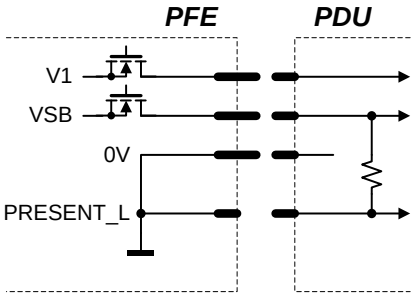


Figure 11. PRESENT_L signal pin

8.5 PSKILL_H INPUT

The PSKILL_H input is active-high and is located on a recessed pin on the connector and is used to disconnect the main output as soon as the power supply is being plugged out. This pin should be connected to SGND in the power distribution unit. The standby output will remain on regardless of the PSKILL_H input state.

8.6 VINOK_H

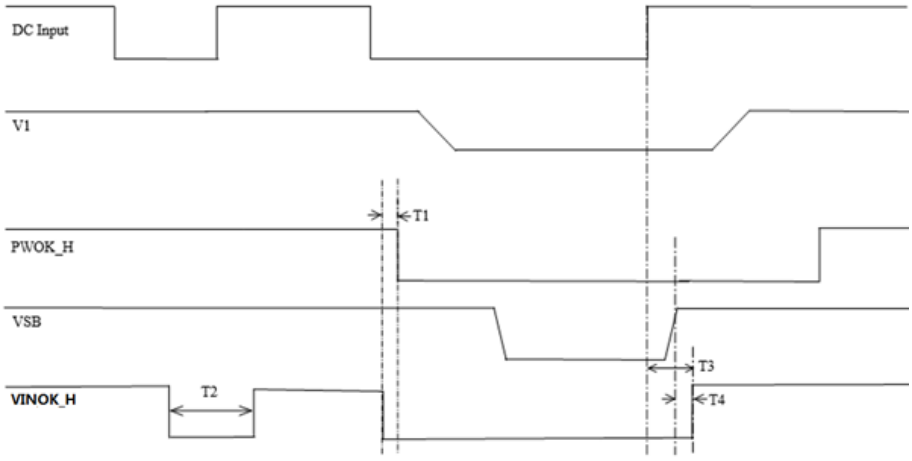


Figure 12. VINOK_H Timing

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
T1	VIN_OK_H & PWOK_H	1			ms
T2	VIN_OK_H Dwell Time	75		120	ms
T3	VIN_OK_H delay to DC			1700	ms
T4	VIN_OK_H to VSB			20	ms

Table 2. VINOK_H Timing Requirement

8.7 TIMING REQUIREMENTS

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits (Tvout_rise) within 1 to 70 ms. All outputs must rise monotonically. *Table 3* shows the timing requirements for the power supply being turned on and off two ways; 1) via the DC input with PSON_L held low; 2) via the PSON_L signal with the DC input applied. The PSU needs to remain off for 1 second minimum after PWOK_H is de-asserted.

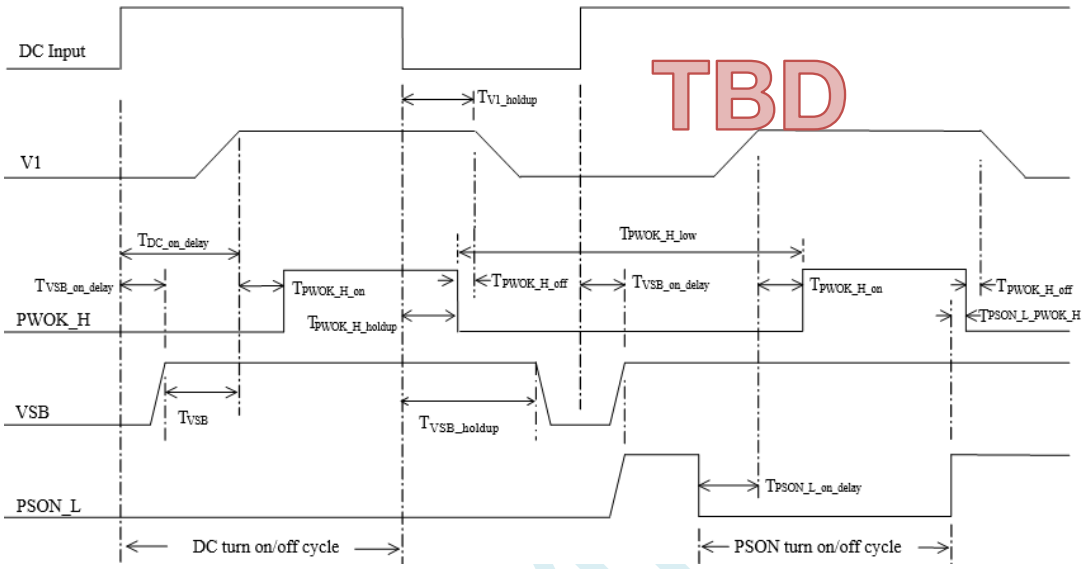


Figure 13. Timing Requirement

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
T_{V1_rise}	Output voltage rise time	1.0		70	ms
$T_{VSB\_on\_delay}$	Delay from DC being applied to VSB being within regulation.			1500	ms
$T_{DC\_on\_delay}$	Delay from DC being applied to all output voltages being within regulation.			3000	ms
T_{V1_holdup}	Time 12 V output voltage stay within regulation after loss of DC.	2			ms
$T_{PWOK\_H\_holdup}$	Delay from loss of DC to de-assertion of PWOK_H	1.5			ms
$T_{PSON\_L\_on\_delay}$	Delay from PSON_L active to output voltages within regulation limits.	5		400	ms
$T_{PSON\_L\_PWOK\_H}$	Delay from PSON_L deactivate to PWOK_H being de-asserted.			5	ms
$T_{PWOK\_H\_on}$	Delay from output voltages within regulation limits to PWOK_H asserted at turn on.	100		500	ms
$T_{PWOK\_H\_off}$	Delay from PWOK_H de-asserted to output voltages dropping out of regulation limits.	0.5			ms
$T_{PWOK\_H\_low}$	Duration of PWOK_H being in the de-asserted state during an off/on cycle using DC or the PSON_L signal.	100			ms
T_{VSB}	Delay from VSB being in regulation to O/Ps being in regulation at DC turn on.	50		1000	ms
T_{VSB_holdup}	Time the VSB output voltage stays within regulation after loss of DC.	10			ms
$T_{DC\_off\_SMB\_ALERT\_L}$	The power supply shall assert the SMB_ALERT_L signal quickly after a loss of DC input voltage.			2	ms

Table 3. Timing Requirement

8.8 CURRENT SHARE

The PFE front-ends have an active current share scheme implemented for V_1. All the ISHARE current share pins need to be interconnected in order to activate the sharing function. If a supply has an internal fault or is not turned on, it will disconnect its ISHARE pin from the share bus. This will prevent dragging the output down (or up) in such cases.

The current share function uses a digital bi-directional data exchange on a recessive bus configuration to transmit and receive current share information. The controller implements a Master/Slave current share function. The power supply providing the largest current among the group is automatically the Master. The other supplies will operate as Slaves and increase their output current to a value close to the Master by slightly increasing their output voltage. The voltage increase is limited to +250 mV. The standby output uses a passive current share method (droop output voltage characteristic).

8.9 SENSE INPUTS

The main output have sense lines implemented to compensate for voltage drop on load wires. The maximum allowed voltage drop is 200 mV on the positive rail and 100 mV on the PGND rail.

With open sense inputs the main output voltage will rise by 270 mV. Therefore, if not used, these inputs should be connected to the power output and PGND close to the power supply connector. The sense inputs are protected against short circuit. In this case the power supply will shut down.

8.10 HOT-STANDBY OPERATION

The hot-standby operation is an operating mode allowing to further increase efficiency at light load conditions in a redundant power supply system. Under specific conditions one of the power supplies is allowed to disable its DC/DC stage. This will save the power losses associated with this power supply and at the same time the other power supply will operate in a load range having a better efficiency. In order to enable the hot standby operation, the HOTSTANDBYEN_H and the ISHARE pins need to be interconnected. A power supply will only be allowed to enter the hot-standby mode, when the HOTSTANDBYEN_H pin is high, the load current is low and the supply was allowed to enter the hot-standby mode by the system controller via the appropriate I^2C command (by default disabled). The system controller needs to ensure that only one of the power supplies is allowed to enter the hot-standby mode.

If a power supply is in a fault condition, it will pull low its active-high HOTSTANDBYEN_H pin which indicates to the other power supply that it is not allowed to enter the hot-standby mode or that it needs to return to normal operation should it already have been in the hot-standby mode.

NOTE: The system controller needs to ensure that only one of the power supplies is allowed to enter the hot-standby model.

Figure 15 shows the achievable power loss savings when using the hot-standby mode operation. A total power loss reduction of 5 W (TBD) is achievable.

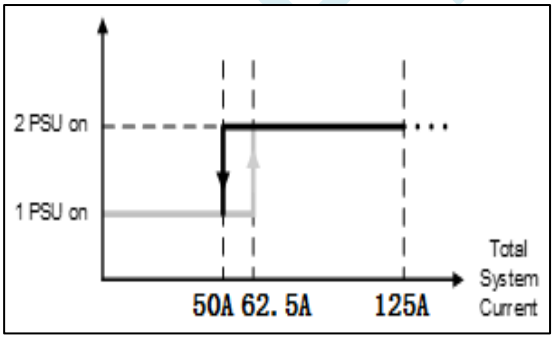


Figure 14. Hot-standby enable/disable current thresholds

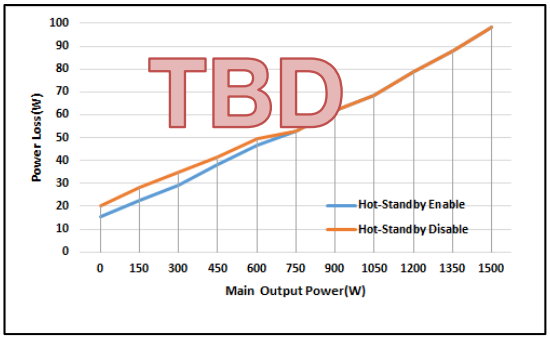


Figure 15. PSU power losses with/without hot-standby mode

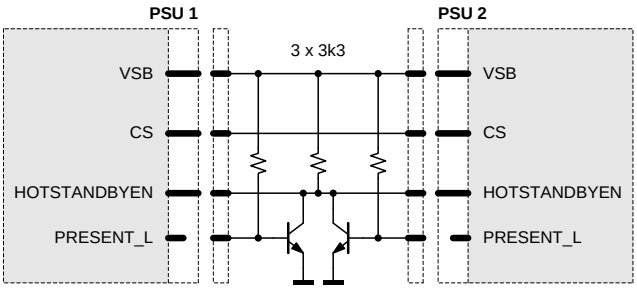


Figure 16. Recommended hot-standby configuration

In order to prevent voltage dips when the active power supply is unplugged while the other is in hot-standby mode, it is strongly recommended to add the external circuit as shown in *Figure 16*. If the PRESENT_L pin status needs also to be read by the system controller, it is recommended to exchange the bipolar transistors with small signal MOS transistors or with digital transistors.

8.11 I²C / SMBUS COMMUNICATION

The interface driver in the PFE supply is referenced to the V1 Return. The PFE supply is a communication Slave device only; it never initiates messages on the I2C/SMBus by itself. The communication bus voltage and timing is defined in *Table 4* further characterized through:

- There are no internal pull-up resistors
- The SDA/SCL IOs are 3.3/5 V tolerant
- Full SMBus clock speed of 100 kbps
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognizes any time Start/Stop bus conditions

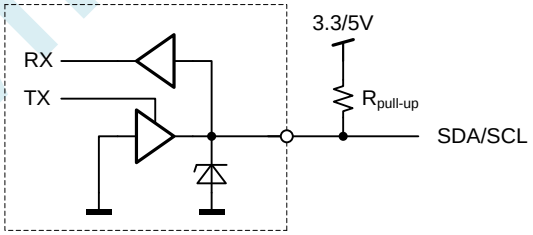


Figure 17. Physical layer of communication interface

The SMB_ALERT_L signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events. The power supply responds to a read command on the general SMB_ALERT_L call address 25(0x19) by sending its status register.

Communication to the DSP or the EEPROM will be possible as long as the input DC voltage is provided. If no DC is present, communication to the unit is possible as long as it is connected to a life V1 output (provided e.g. by the redundant unit). If only VSB is provided, communication is not possible.

PARAMETER	DESCRIPTION / CONDITION		MIN	NOM	MAX	UNIT
V_{iL}	Input low voltage		-0.5		1.0	V
V_{iH}	Input high voltage		2.3		5.5	V
V_{hys}	Input hysteresis		0.15			V
V_{oL}	Output low voltage	3 mA sink current	0		0.4	V
t_r	Rise time for SDA and SCL		20+0.1Cb[2]		300	Ns
t_{of}	Output fall time ViHmin → ViLmax	10 pF < Cb[2] < 400 pF	20+0.1Cb[2]		250	Ns
I_i	Input current SCL/SDA	0.1 VDD < Vi < 0.9 VDD	-10		10	µA
C_i	Internal Capacitance for each SCL/SDA				50	pF
f_{SCL}	SCL clock frequency		0		100	kHz
R_{pu}	External pull-up resistor	f_{SCL} ≤ 100 kHz			1000 ns / Cb	Ω
t_{HDSTA}	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	4.0			µs
t_{LOW}	Low period of the SCL clock	f_{SCL} ≤ 100 kHz	4.7			µs
t_{HIGH}	High period of the SCL clock	f_{SCL} ≤ 100 kHz	4.0			µs
t_{SUSTA}	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	4.7			µs
t_{HDDAT}	Data hold time	f_{SCL} ≤ 100 kHz	0		3.45	µs
t_{SUDAT}	Data setup time	f_{SCL} ≤ 100 kHz	250			ns
t_{SUSTO}	Setup time for STOP condition	f_{SCL} ≤ 100 kHz	4.0			µs
t_{BUF}	Bus free time between STOP and START	f_{SCL} ≤ 100 kHz	5			ms

Table 4. I2C / SMBus Specification

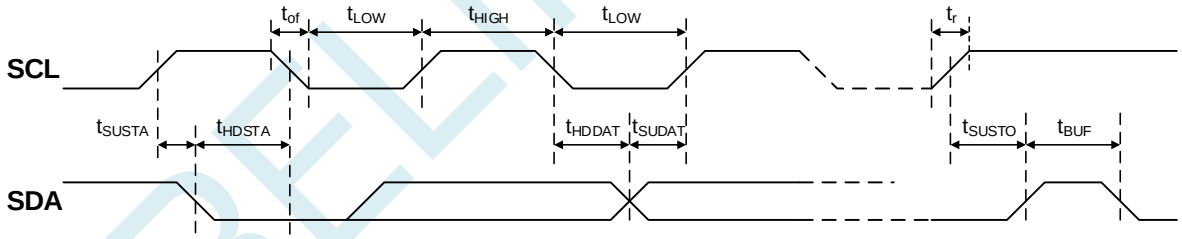


Figure 18. I2C / SMBus Timing

[2] Cb = Capacitance of bus line in pF, typically in the range of 10…400 pF

8.12 ADDRESS / PROTOCOL SELECTION (APS)

The APS pin provides the possibility to select the address by connecting a resistor to V1 return (0 V). A fixed addressing offset exists between the Controller and the EEPROM.

NOTES:

- If the APS pin is left open, the supply will operate with the Power Management Bus protocol at controller / EEPROM addresses 0xB6 / 0xA6.
- The APS pin is only read at start-up of the power supply. Therefore, it is not possible to change address dynamically.

R_{APS} (Ω) [3]	Protocol	I2C Address [4]	
		Controller	EEPROM
820	Power Management Bus	0xB0	0xA0
2700		0xB2	0xA2
5600		0xB4	0xA4
8200		0xB6	0xA6

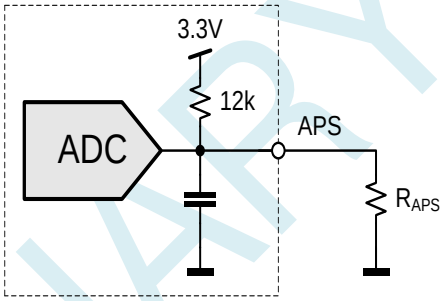


Figure 19. I2C address and protocol setting

8.13 CONTROLER AND EEPROM ACCESS

The controller and the EEPROM in the power supply share the same I2C bus physical layer (see *Figure 20*). An I2C driver device assures logic level shifting (3.3/5 V) and a glitch-free clock stretching. The driver also pulls the SDA/SCL line to nearly 0 V when driven low by the DSP or the EEPROM providing maximum flexibility when additional external bus repeaters are needed. Such repeaters usually encode the low state with different voltage levels depending on the transmission direction.

The DSP will automatically set the I2C address of the EEPROM with the necessary offset when its own address is changed / set. In order to write to the EEPROM, first the write protection needs to be disabled by sending the appropriate command to the DSP. By default, the write protection is on.

The EEPROM provides 256 bytes of user memory. None of the bytes are used for the operation of the power supply.

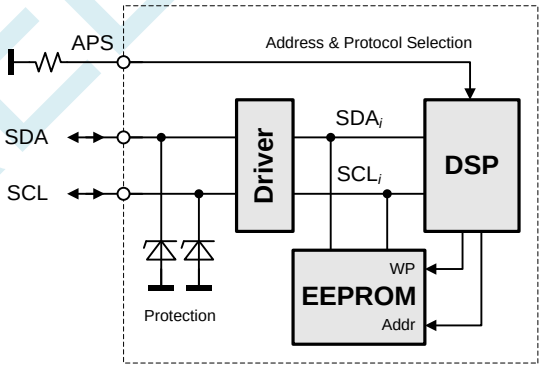


Figure 20. I2C Bus to DPS and EEPROM

[3] E12 resistor values, use max 5% resistors, see also *Figure 19*

[4] The LSB of the address byte is the R/W bit

8.14 EEPROM PROTOCOL

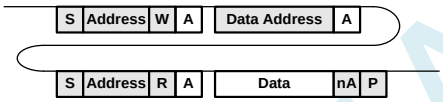
The EEPROM follows the industry communication protocols used for this type of device. Even though page write / read commands are defined, it is recommended to use the single byte write / read commands.

WRITE

The write command follows the SMBus 1.1 Write Byte protocol. After the device address with the write bit cleared a first byte with the data address to write to is sent followed by the data byte and the STOP condition. A new START condition on the bus should only occur after 5ms of the last STOP condition to allow the EEPROM to write the data into its memory.

READ

The read command follows the SMBus 1.1 Read Byte protocol. After the device address with the write bit cleared the data address byte is sent followed by a repeated start, the device address and the read bit set. The EEPROM will respond with the data byte at the specified location.



8.15 POWER MANAGEMENT BUS PROTOCOL

POWER MANAGEMENT BUS PROTOCOL

The Power Management Bus is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at www.powerSIG.org.

Power Management Bus command codes are not register addresses. They describe a specific command to be executed.

The PFE1500-12-054 supply supports the following basic command structures:

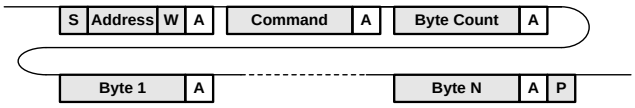
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognized any time Start/Stop bus conditions

WRITE

The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).

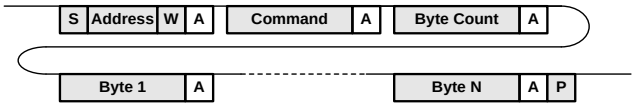
1) Optional

In addition, Block write commands are supported with a total maximum length of 255 bytes. See PFE Programming Manual for further information.

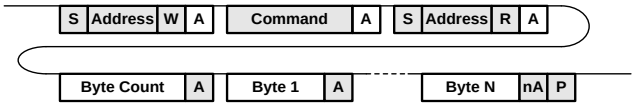


READ

The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.



In addition, Block read commands are supported with a total maximum length of 255 bytes. See PFE Programming Manual BCA.00006 for further information.



8.16 GRAPHICAL USER INTERFACE

Bel Power Solutions provide with its “Bel Power Solutions I2C Utility” a Windows® XP/Vista/Win7 compatible graphical user interface allowing the programming and monitoring of the PFE1500-12-054xD Front-End. The utility can be downloaded on: belfuse.com/power-solutions and supports Power Management Bus protocols.

The GUI allows automatic discovery of the units connected to the communication bus and will show them in the navigation tree. In the monitoring view the power supply can be controlled and monitored.

If the GUI is used in conjunction with the SNP-OP-BOARD-01 or YTM.G1Q01.0 Evaluation Kit it is also possible to control the PSON_L pin(s) of the power supply.

Further there is a button to disable the internal fan for approximately 10 seconds. This allows the user to take input power measurements without fan consumptions to check efficiency compliance to the Climate Saver Computing Platinum specification.

The monitoring screen also allows to enable the hot-standby mode on the power supply. The mode status is monitored and by changing the load current it can be monitored when the power supply is being disabled for further energy savings. This obviously requires 2 power supplies being operated as a redundant system (as in the evaluation kit).

NOTE: The user of the GUI needs to ensure that only one of the power supplies have the hot-standby mode enabled.

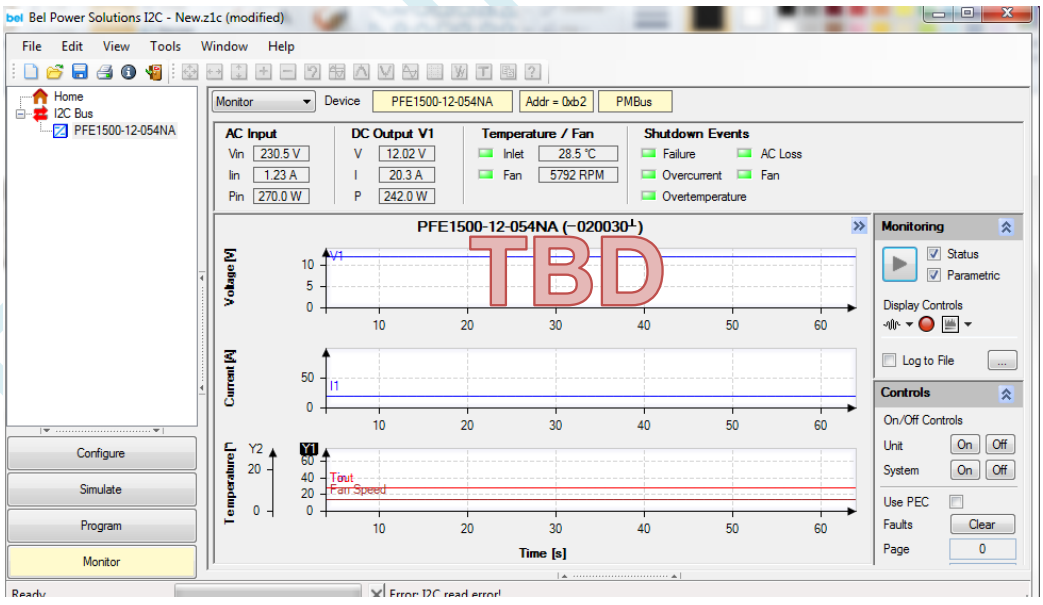


Figure 21. Monitoring dialog of the I2C Utility

9. TEMPERATURE AND FAN CONTROL

To achieve best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the airflow at the rear of the supply by placing large objects directly at the output connector. The PFE1500-12NDS412 is provided with normal airflow, which means the air enters through the DC-output of the supply and leaves at the DC input connector. PFE supplies have been designed for horizontal operation.

The fan inside of the supply is controlled by a microprocessor. The RPM of the fan is adjusted to ensure optimal supply cooling and is a function of output power and the inlet temperature.

For the normal airflow version additional constraints apply because of the DC-connector. In a normal airflow unit, the hot air is exiting the power supply unit at the DC-inlet.

NOTE: It is the responsibility of the user to check the front temperature in such cases. The unit is not limiting its power automatically to meet such a temperature limitation.

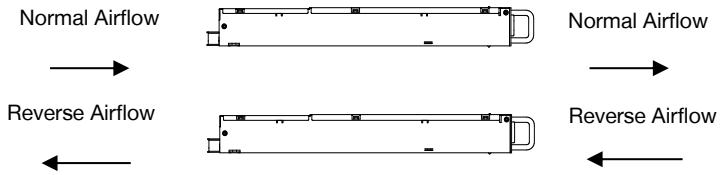


Figure 22. Airflow direction

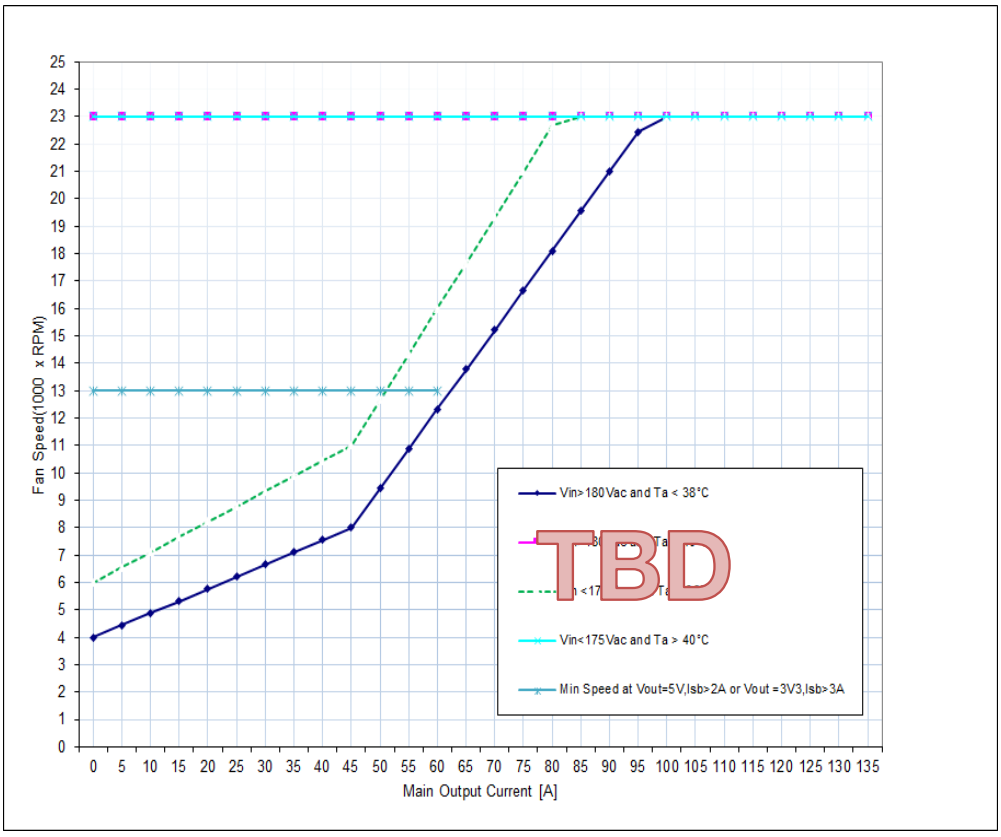


Figure 23. Fan speed vs. main output load

10. ELECTROMAGNETIC COMPATIBILITY

10.1 IMMUNITY

NOTE: Most of the immunity requirements are derived from EN 55024:2010/A1:2015.

TEST	STANDARD / DESCRIPTION	CRITERIA
ESD Contact Discharge	IEC / EN 61000-4-2, ±8 kV, 25+25 discharges per test point (metallic case, LEDs, connector body)	B
ESD Air Discharge	IEC / EN 61000-4-2, ±15 kV, 25+25 discharges per test point (non-metallic user accessible surfaces)	B
Radiated Electromagnetic Field	EN 55024: 2010/A1: 2015 using the IEC 61000-4-3: 2002-09 test standard and performance criteria A defined in Annex B of CISPR 24	A
Burst	IEC / EN 61000-4-4, level 3 Input DC port ±1 kV, 1 minute DC port ±0.5 kV, 1 minute	B
Surge	IEC / EN 61000-4-5 Line to earth: ±1 kV Line to line: ±0.5 kV	B
RF Conducted Immunity	IEC/EN 61000-4-6, Level 3, 10 Vrms, CW, 0.1 … 80 MHz	A

10.2 EMISSION

TEST	STANDARD / DESCRIPTION	CRITERIA
Conducted Emission	EN55032 / CISPR 32: 0.15 … 30 MHz, QP and AVG, single unit, V_i = 53 VDC, $P_{x\,nom}$	Class A
	EN55032 / CISPR 32: 0.15 … 30 MHz, QP and AVG, 2 units in rack system, V_i = 53 VDC, $P_{x\,nom}$	Class A
Radiated Emission	EN55032 / CISPR 32: 30 MHz … 1 GHz, QP, single unit, V_i = 53 VDC, $P_{x\,nom}$	Class A
	EN55032 / CISPR 32: 30 MHz … 1 GHz, QP, 2 units in rack system, V_i = 53 VDC, $P_{x\,nom}$	Class A
Acoustical Noise	Sound power statistical declaration (ISO 9296, ISO 7779, IS9295) @ 50% load & 25°C	62 dBA

11. ENVIRONMENTAL SPECIFICATIONS

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
T_A	Ambient Temperature	$V_{i\,min}$ to $V_{i\,max}$, $I_{o\,nom}$, $I_{SB\,nom}$	0		+45	°C
T_{Aext}	Extended Temp. Range	Derated output	+45		+65	°C
T_S	Storage Temperature	Non-operational	-20		+70	°C
N_a	Audible Noise	Sound power @ $V_{i\,nom}$, 50% $I_{o\,nom}$, T_A = 25°C		62		dBA

12. MECHANICAL SPECIFICATIONS

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
	Dimensions	Width		54.5		mm
		Height		40.0		
		Depth		321.5		
M	Weight			1.13		kg

NOTE: Tolerance (unless otherwise stated): 0-30 mm: +/- 0.2 mm; 30-120 mm: +/- 0.4 mm; 120-400 mm: +/-0.6 mm
NOTES: A 3D step file of the power supply casing is available on request.
Unlatching the supply is performed by pulling the green trigger in the handle

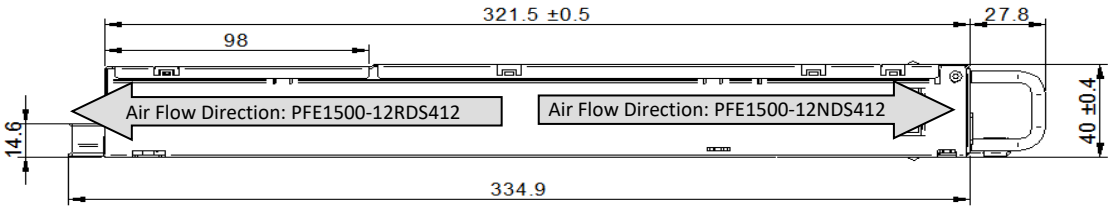


Figure 24. Side View 1

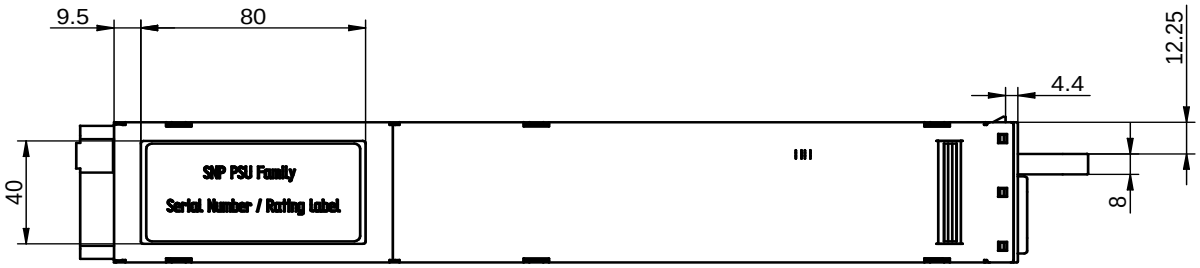


Figure 25. Top View

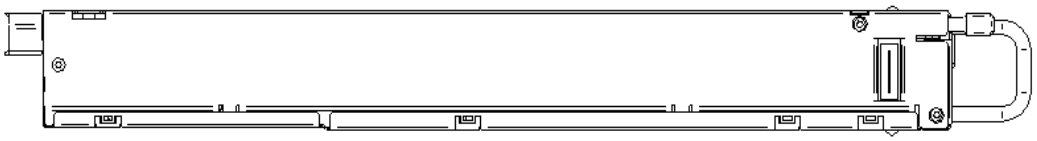


Figure 26. Side View 2

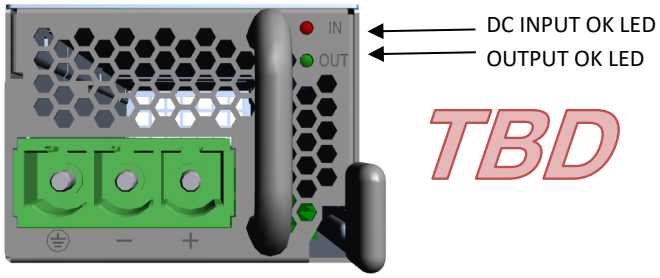
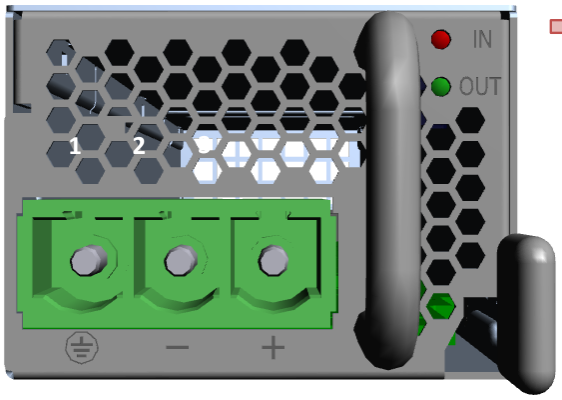


Figure 27. Front View (PFE1500-12-054xD)

13. CONNECTIONS

13.1 INPUT CONNECTOR

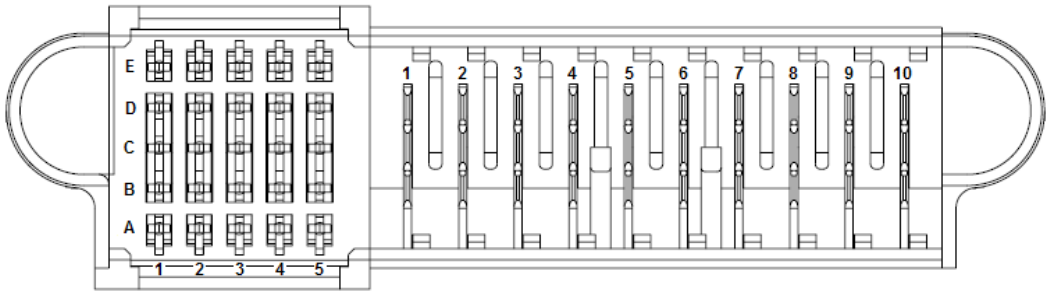


TBD

PIN	NAME	DESCRIPTION
Input		
1	Vin+	Input positive
2	Vin-	Input negative
3	PE	Ground ⏚

Unit: Three pole Phoenix Contact (P/N PC 6-16/ 3-G1-10,16, Code 1998946)
Counter part: Three pole Phoenix Contact (P/N SPC 16/ 3-ST-10,16, Code 1711271) with push-in spring connection (no tools required)

13.2 OUTPUT CONNECTOR

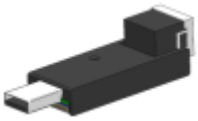
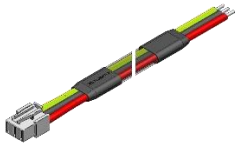
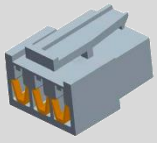


Power Supply Connector: Tyco Electronics P/N 2-1926736-3 **(NOTE: Column 5 is recessed (short pins))**
Mating Connector: Tyco Electronics P/N 2-1926739-5 or FCI 10108888-R10253SLF

PIN	NAME	DESCRIPTION
Output		
6, 7, 8, 9, 10	V1	+12 VDC main output
1, 2, 3, 4, 5	PGND	Power ground (return)
Control Pins		
A1	VSB	Standby positive output (+3.3/5 V_{SB} or 12 V_{SB})
B1	VSB	Standby positive output (+3.3/5 V_{SB} or 12 V_{SB})
C1	VSB	Standby positive output (+3.3/5 V_{SB} or 12 V_{SB})
D1	VSB	Standby positive output (+3.3/5 V_{SB} or 12 V_{SB})
E1	VSB	Standby positive output (+3.3/5 V_{SB} or 12 V_{SB})
A2	SGND	Signal ground (return)
B2	SGND	Signal ground (return)
C2	HOTSTANDBYEN_H	Hot standby enable signal: active-high
D2	VSB_SENSE_R	Standby output negative sense **(Not used for 12 V_{SB} model)**
E2	VSB_SENSE	Standby output positive sense **(Not used for 12 V_{SB} model)**
A3	APS	I^2C address and protocol selection (select by a pull down resistor)
B3	N/C	Reserved
C3	SDA	I^2C data signal line
D3	V1_SENSE_R	Main output negative sense
E3	V1_SENSE	Main output positive sense
A4	SCL	I^2C clock signal line
B4	PSON_L	Power supply on input (connect to A2/B2 to turn unit on): active-low
C4	SMB_ALERT_L	SMB Alert signal output: active-low
D4	N/C	Reserved
E4	VINOK_H	DC input OK signal: active-high
A5	PSKILL_H	Power supply kill (lagging pin): active-high
B5	ISHARE	Current share bus (lagging pin)
C5	PWOK_H	Power OK signal output (lagging pin): active-high
D5	VSB_SEL	Standby voltage selection (lagging pin) **(Not used for 12 V_{SB} model)**
E5	PRESENT_L	Power supply present (lagging pin): active-low

Table 5. Pin Description

14. ACCESSORIES

ITEM	DESCRIPTION	ORDERING PART NUMBER	SOURCE
	**I²C Utility** Windows XP/Vista/7 compatible GUI to program, control and monitor PFE Front-Ends (and other I²C units)	N/A	belfuse.com/power-solutions
	**USB to I²C Converter** Master I²C device to program, control and monitor I²C units in conjunction with the *I²C Utility*	ZM-00056	Bel Power Solutions
	**Dual Connector Board** Connector board to operate 2 PFE units in parallel. Includes an on-board USB to I²C converter (use *I²C Utility* as desktop software)	SNP-OP-BOARD-01 YTM.G1Q01.0	Bel Power Solutions
	**Cable Harness with Mating input Connector** CHINA AVIATION , PN: DP5TJY0300-001, 2.44m length, 10AWG wire with 10mm stripping at the end, encased with braided sleeving	ZLH.00742	Bel Power Solutions
	**Female Pin Connector Terminal** Spare Mating Connectors	ZES.00046	Bel Power Solutions

15. REVISION HISTORY

DATE	REVISION	SECTION	ISSUE	PREPARED BY	APPROVED BY
2018/01/18	001	/	First release	Baker Xu	Mike Chen
2018/03/22	002		Information for PN with 3.3/5Vsb added		
2019/04/02	003		Power Management Bus wording update		

For more information on these products consult: tech.support@psbel.com

NUCLEAR AND MEDICAL APPLICATIONS - Products are not designed or intended for use as critical components in life support systems, equipment used in hazardous environments, or nuclear control systems.
TECHNICAL REVISIONS - The appearance of products, including safety agency certifications pictured on labels, may change depending on the date manufactured. Specifications are subject to change without notice.